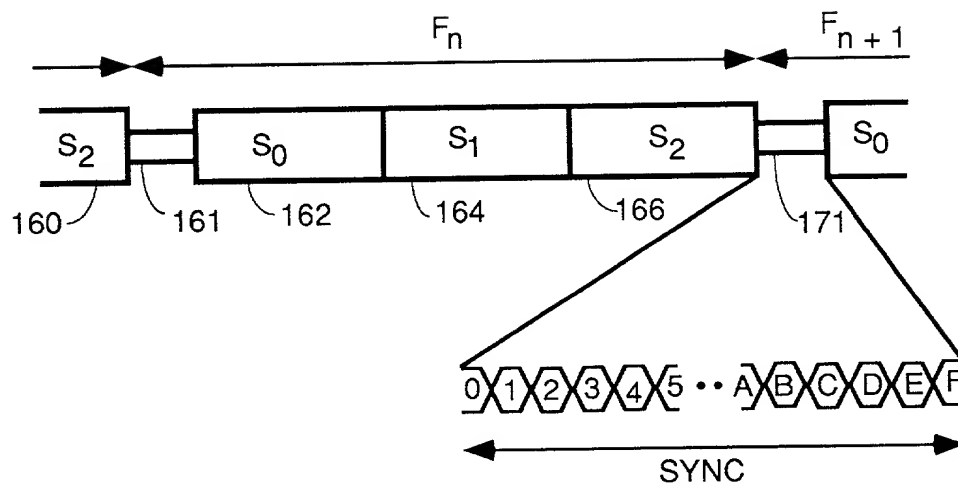


FIG. 1

#6



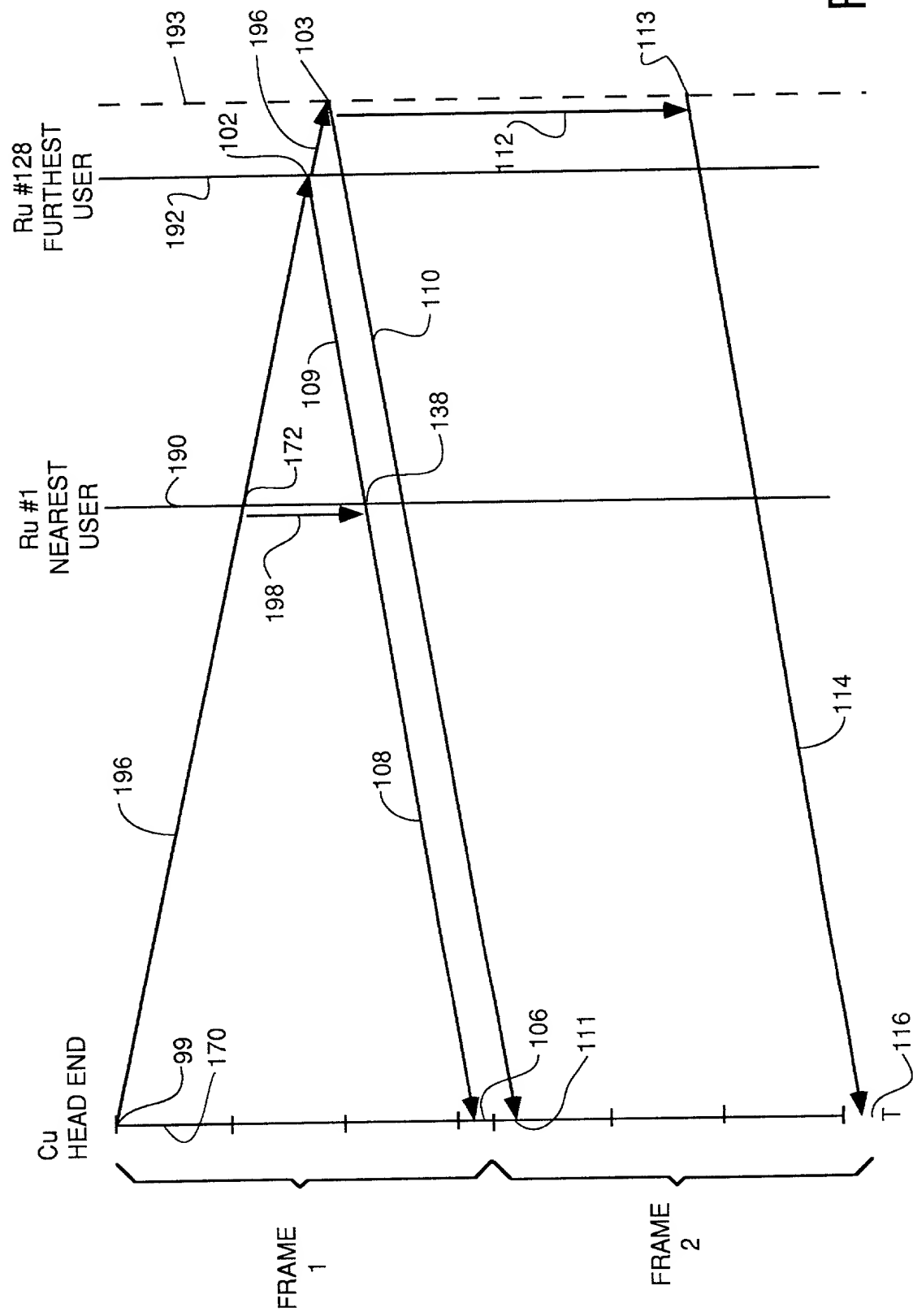


FIG. 3

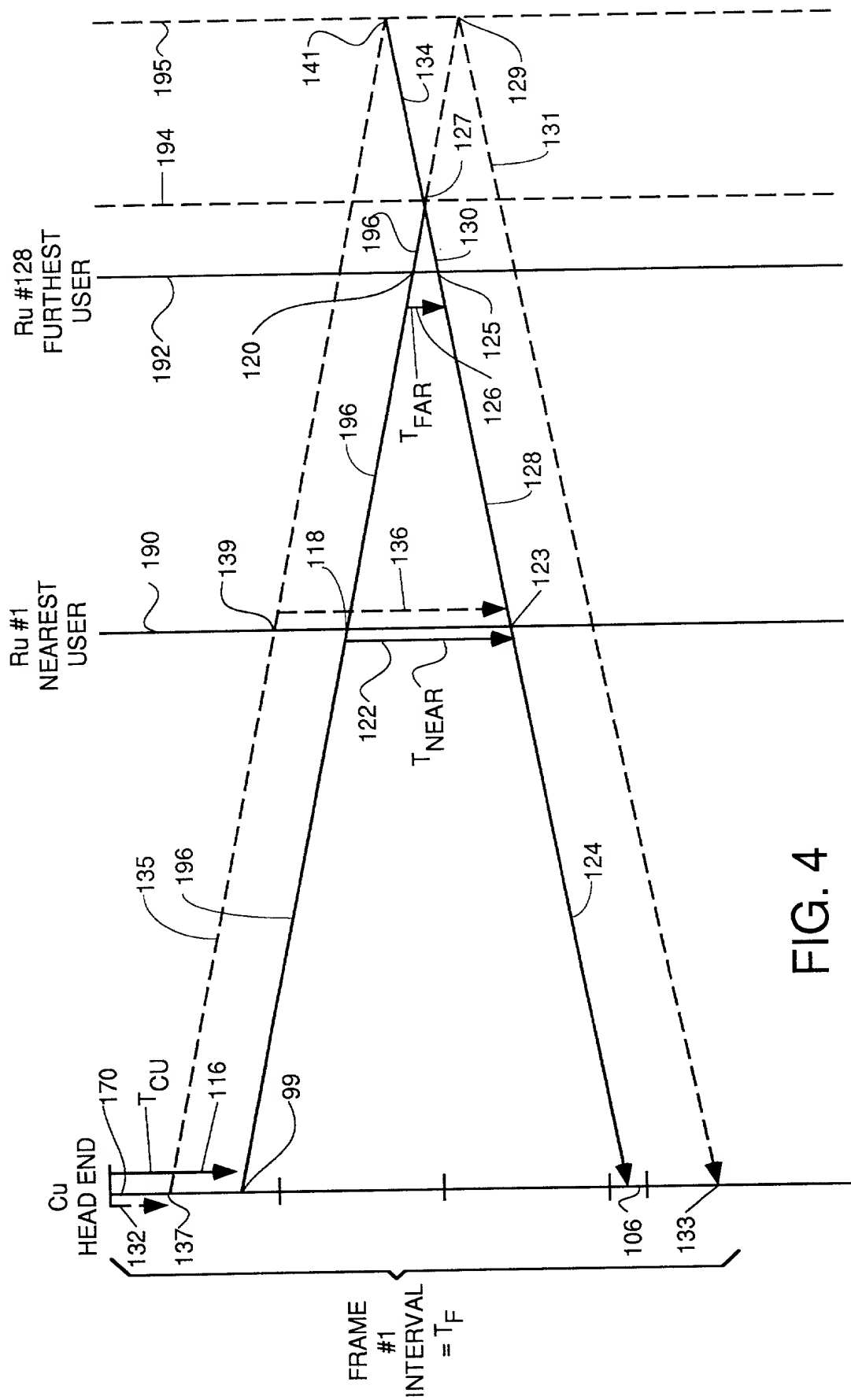
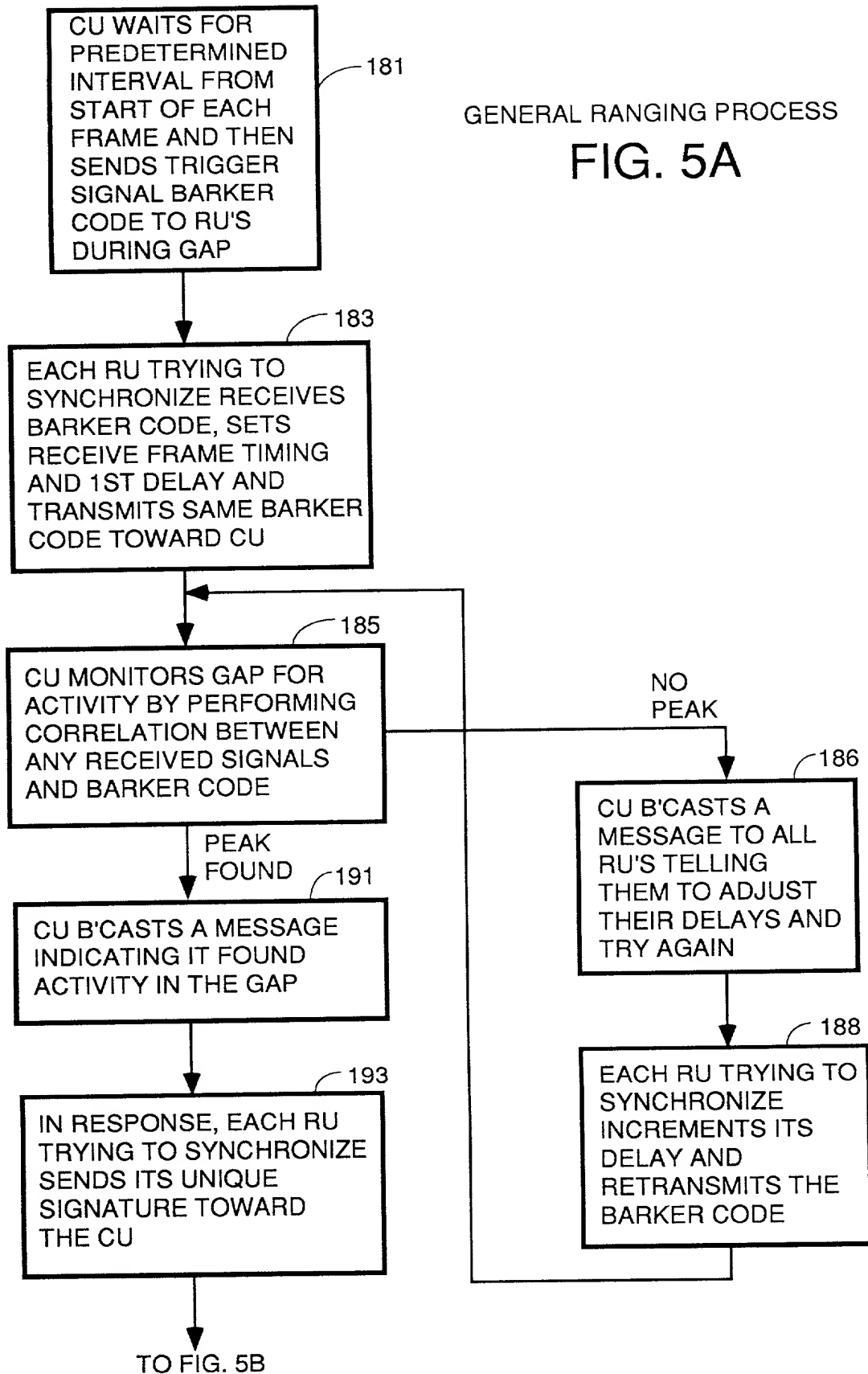


FIG. 4

GENERAL RANGING PROCESS

FIG. 5A



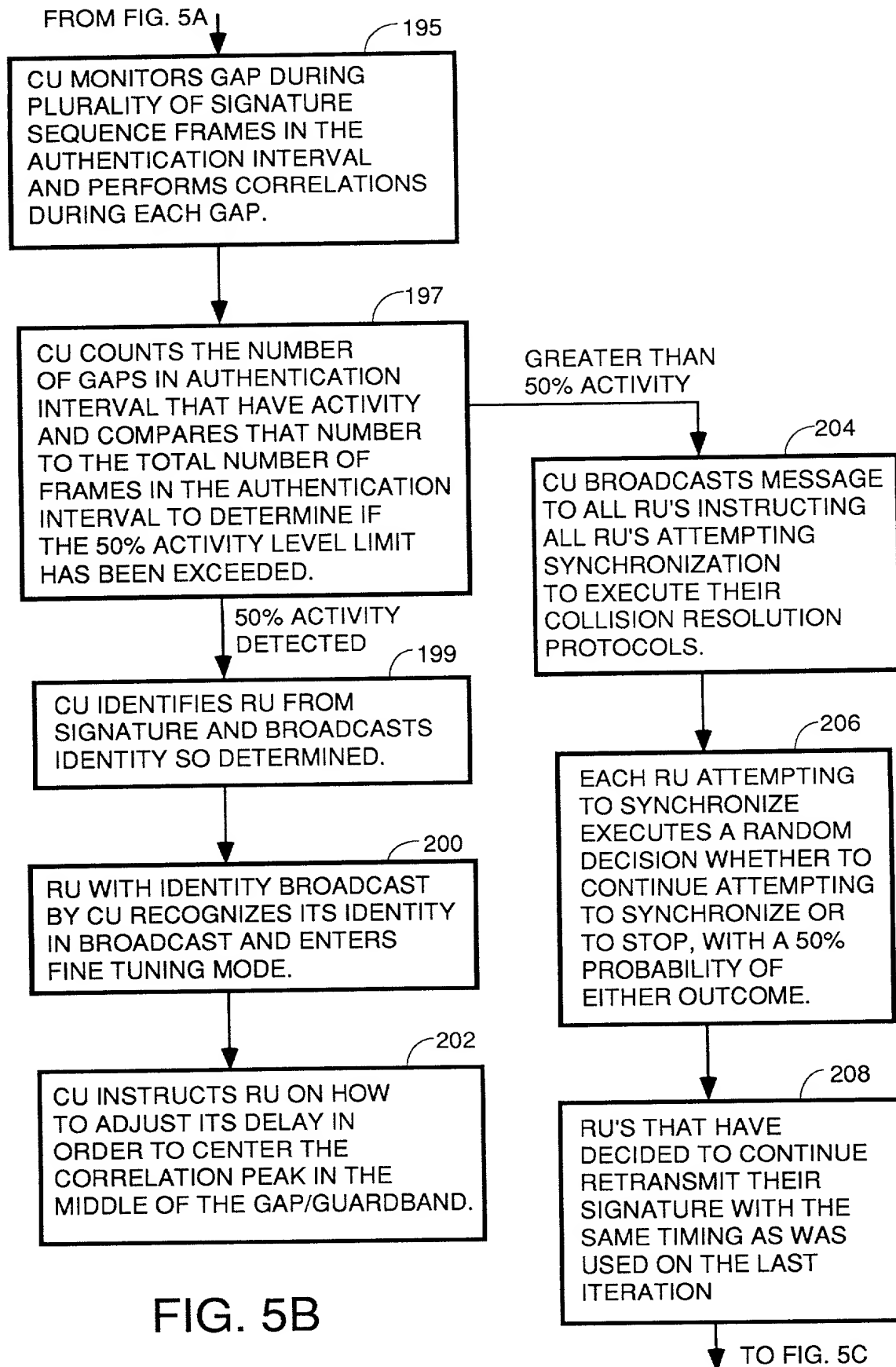


FIG. 5B

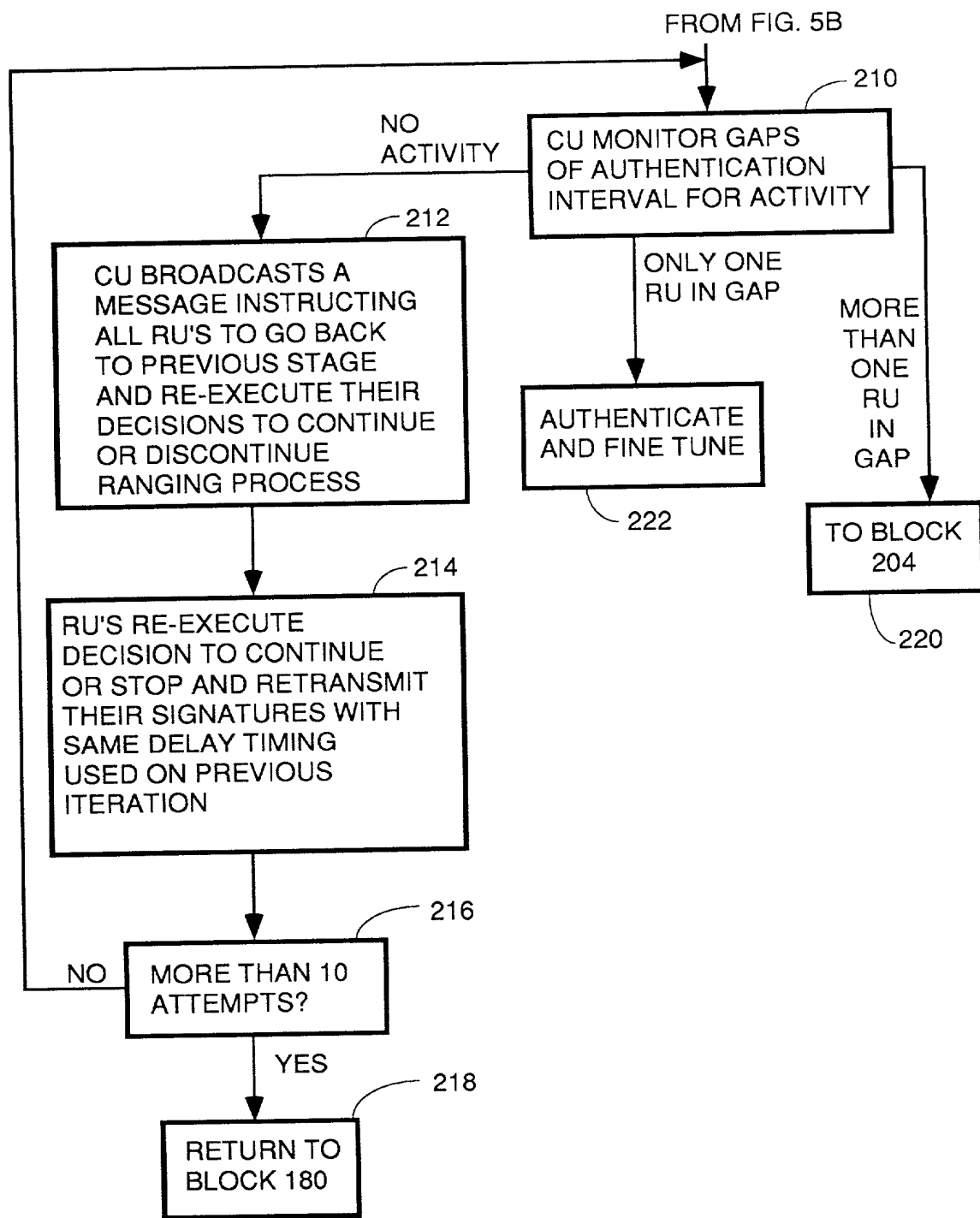


FIG. 5C

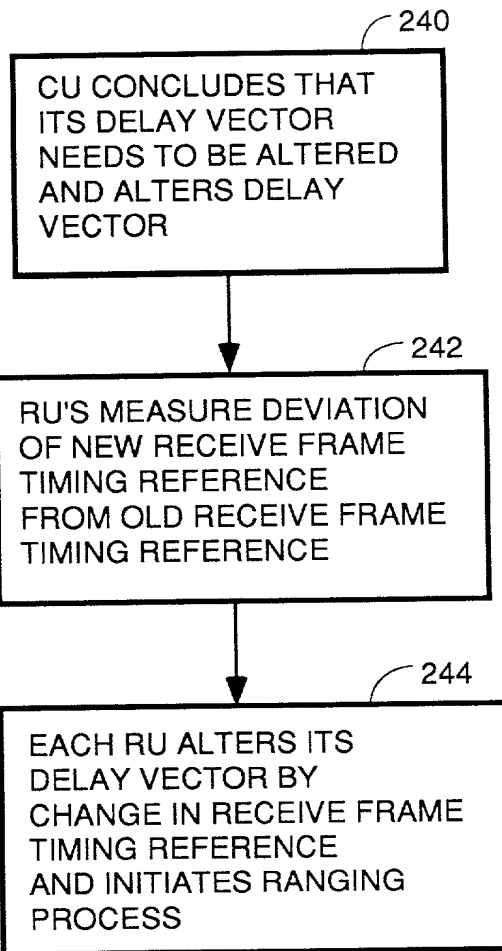


FIG. 6
DEAD RECKONING RE-SYNC

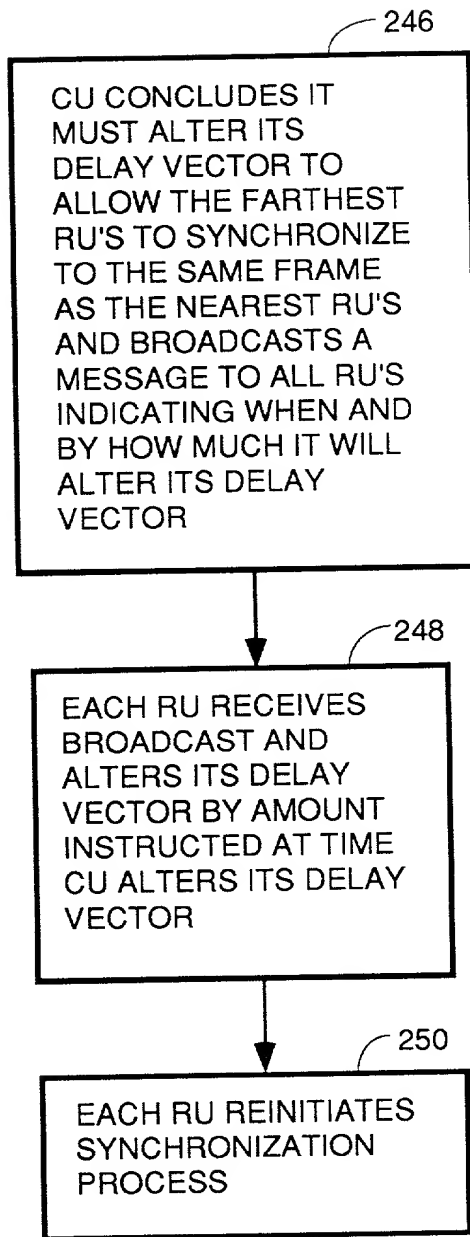


FIG. 7
PRECURSOR EMBODIMENT



FIG. 8

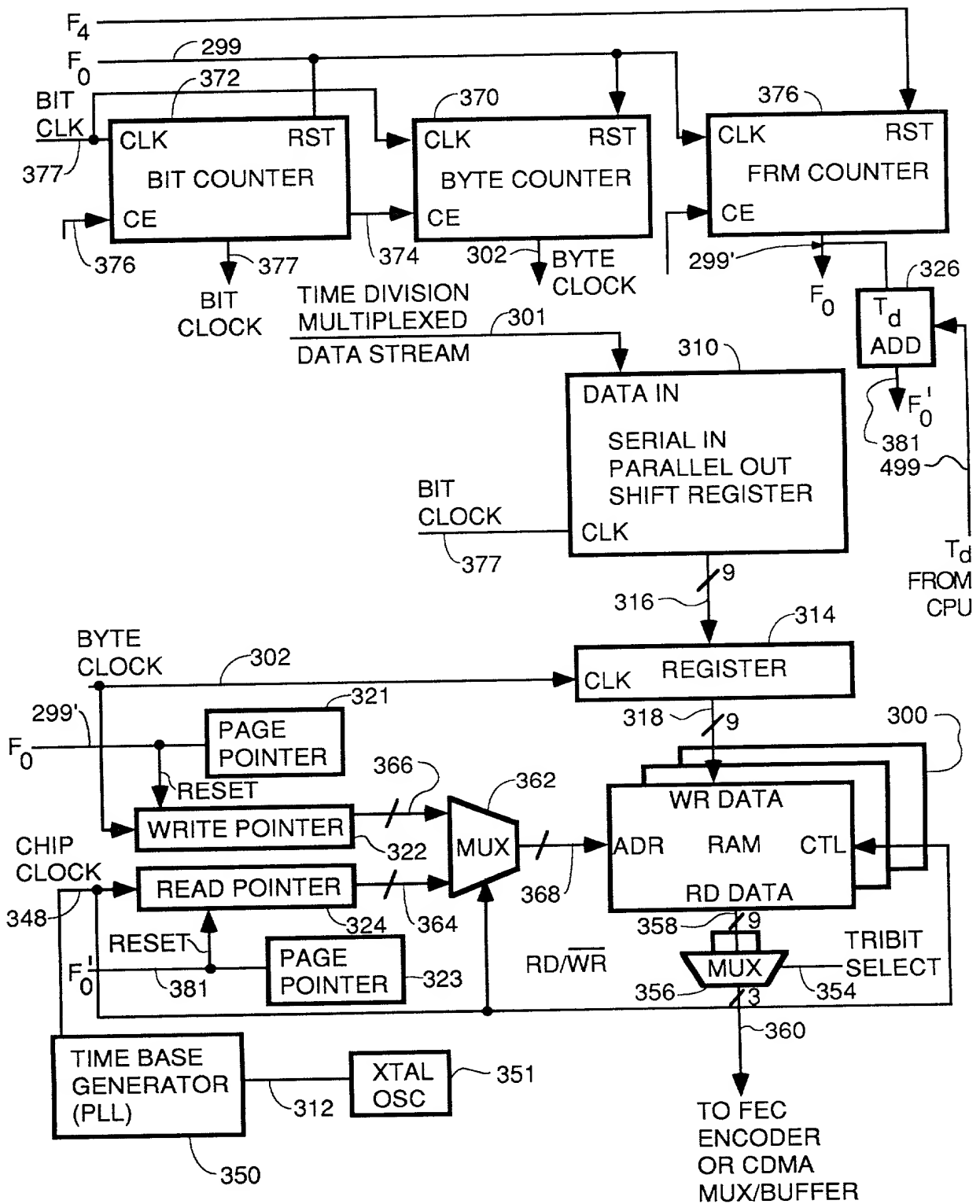


FIG. 9

Timing diagram showing nine signals (T1-T9) related to clock and data strobes:

- T1: CHIP CLK (F_s) with period T_c .
- T2: BIT CLK ($16/7 F_s$) with period T_b .
- T3: BYTE CLK ($2/7 F_s$) with period T_s .
- T4: A step function.
- T5: A high-frequency signal labeled $16 \times F_s$.
- T6: A signal labeled $2 \times F_s$.
- T7: A signal labeled F_s with period T_c .
- T8: A signal labeled $16/7 F_s$ with period T_b .
- T9: A signal labeled T_s with period T_s .

FIG. 10

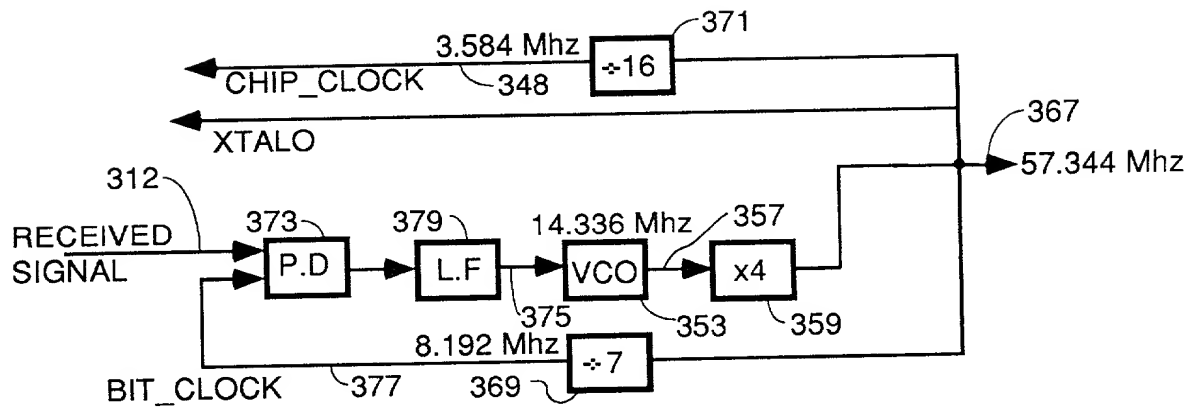


FIG. 11

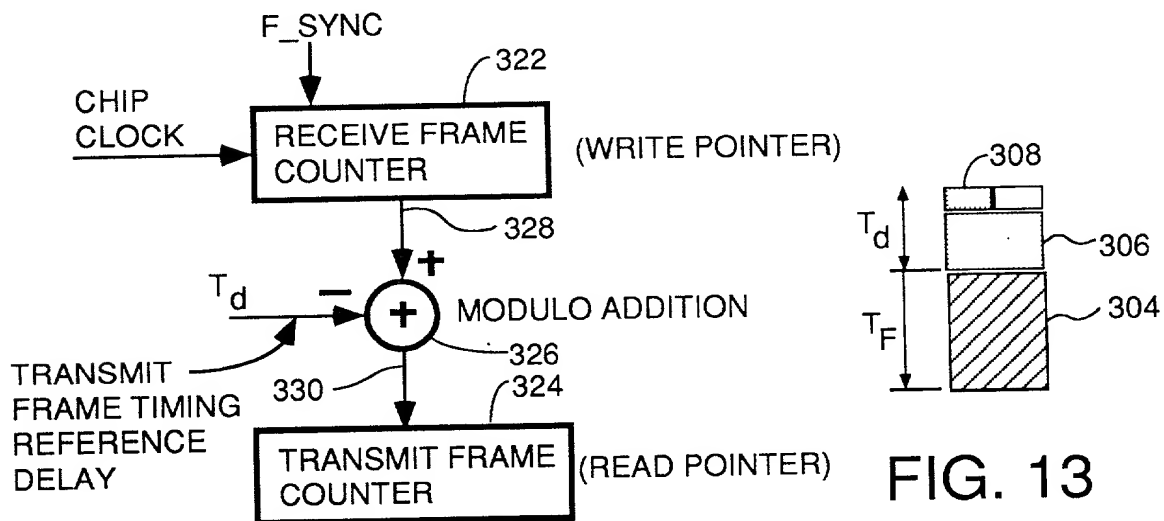


FIG. 12

FIG. 13

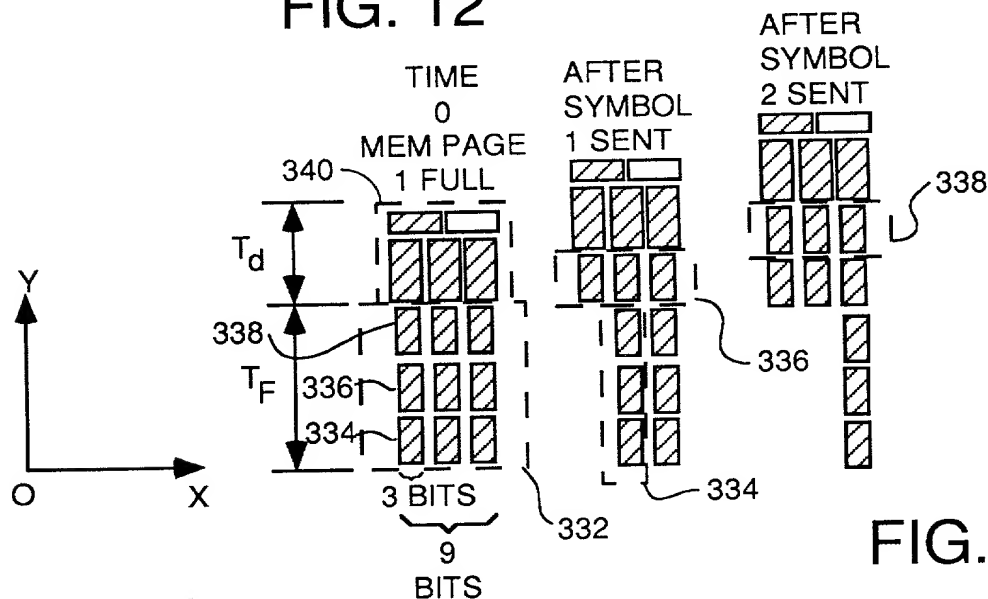


FIG. 14

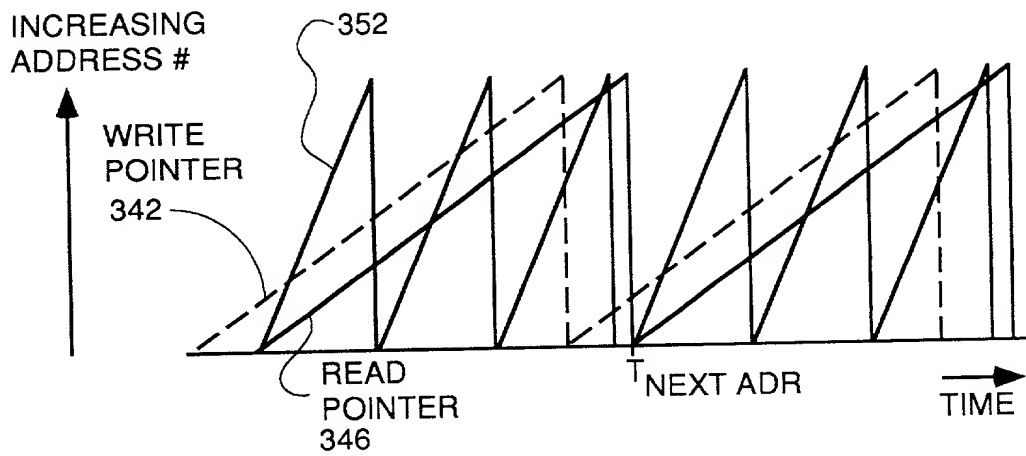


FIG. 15

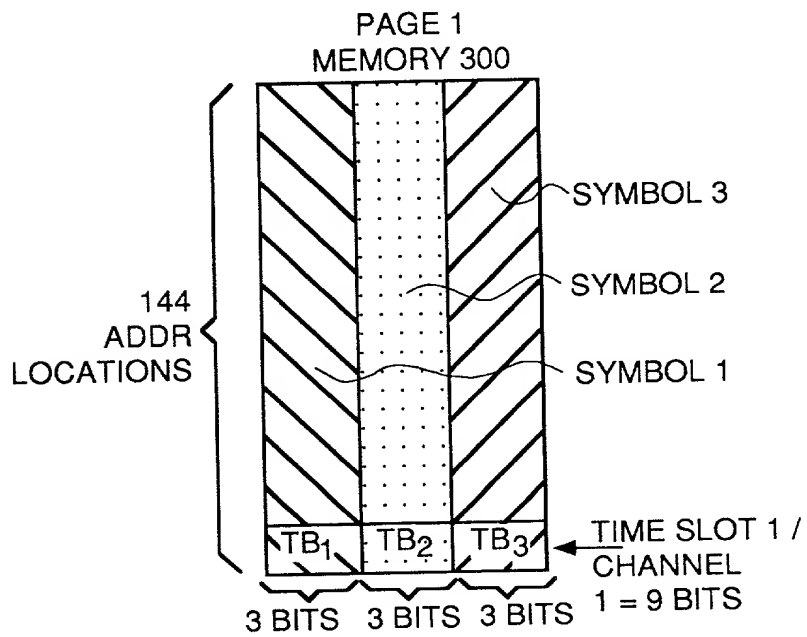
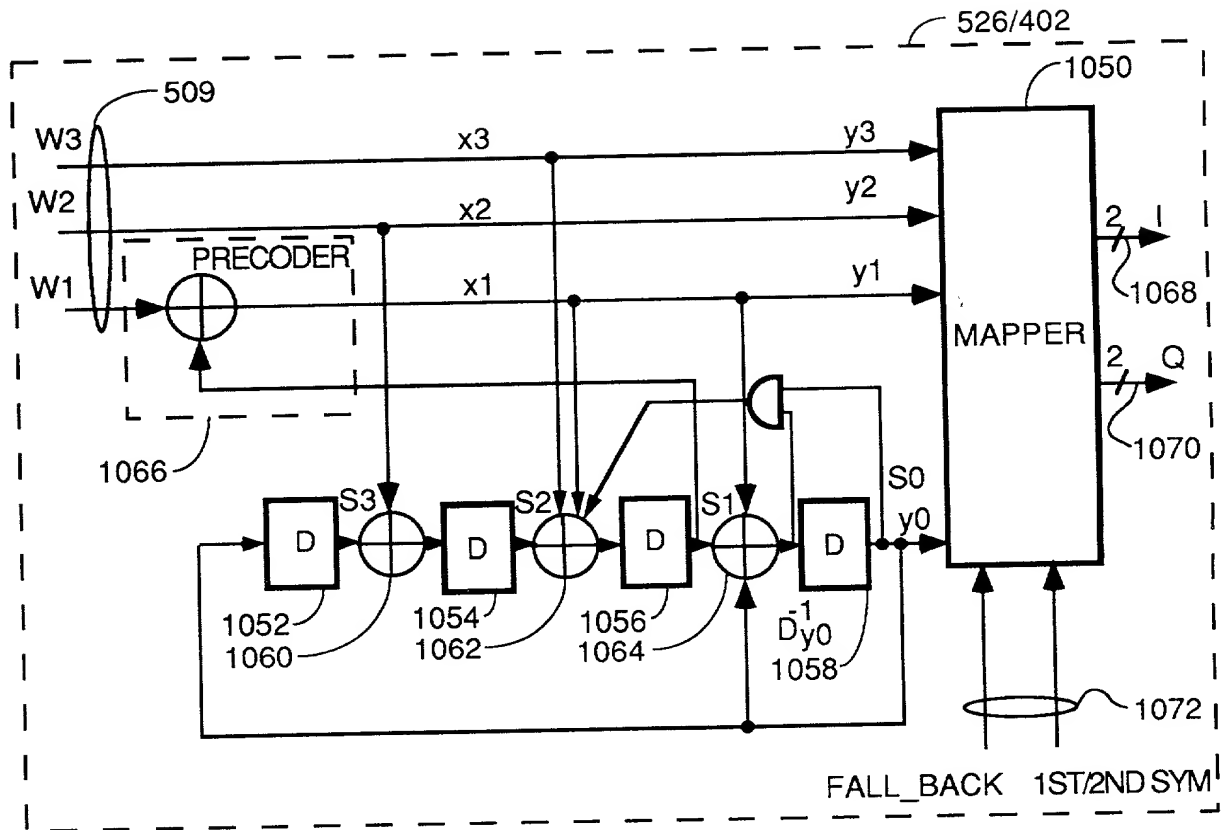


FIG. 16

FIG. 17



PREFERRED TRELLIS ENCODER
FIG. 17

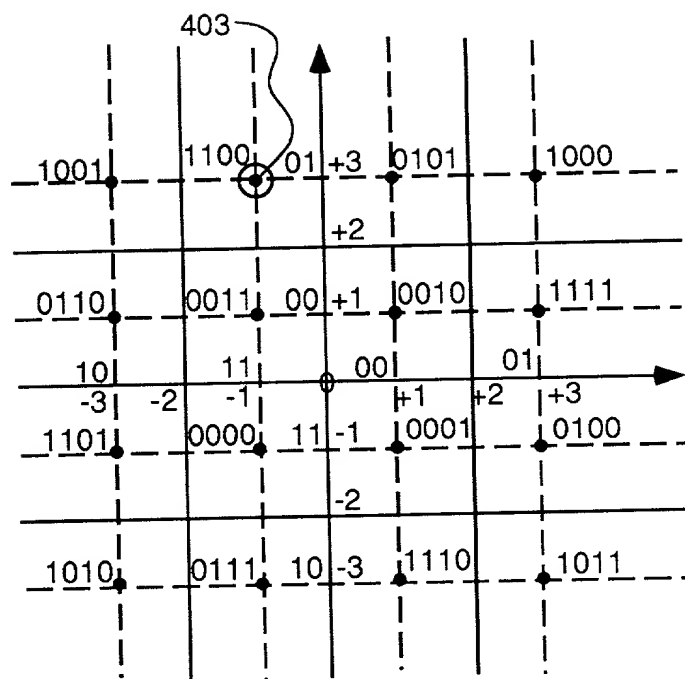


FIG. 18

0000	111	111	
0001	001	111	= 1 - j
0010	001	001	= 1 + j
0011	111	001	= -1 + j
0100	011	111	= 3 - j
0101	001	011	= 1 + 3*j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3*j
1000	011	011	= +3 + 3*j
1001	101	011	= -3 + 3*j
1010	101	101	= -3 - 3*j
1011	011	101	= 3 - 3*j
1100	111	011	= -1 + 3*j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3*j
1111	011	001	= 3 + j

FIG. 19

INFORMATION
VECTOR [B]
FOR EACH
SYMBOL

ORTHOGONAL
CODE MATRIX

$$\begin{array}{c} 483 \\ 481 \end{array} \begin{bmatrix} 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \\ 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ \vdots & & & \end{bmatrix} \times \begin{bmatrix} C_{1,1} & C_{1,2} & \dots & C_{1,144} \\ C_{2,1} & C_{2,2} & \dots & C_{2,144} \\ \vdots & \vdots & & \vdots \end{bmatrix}$$

FIG. 20A

$$\begin{array}{c} \text{REAL} \\ \text{PART OF} \\ \text{INFO} \\ \text{VECTOR} \\ [b] \text{ FOR} \\ \text{FIRST} \\ \text{SYMBOL} \end{array} \begin{array}{c} 405 \\ \begin{bmatrix} +3 \\ -1 \\ -1 \\ +3 \end{bmatrix} \end{array} \cdot \begin{array}{c} 407 \\ \begin{bmatrix} 1 & 1 & 1 & 1 \\ -1 & -1 & 1 & 1 \\ -1 & 1 & -1 & 1 \\ -1 & 1 & 1 & -1 \end{bmatrix} \end{array} = \begin{array}{c} \text{REAL} \\ \text{PART OF} \\ \text{RESULT} \\ \text{VECTOR} \end{array} \begin{array}{c} 409 \\ \begin{bmatrix} 4 \\ 0 \\ 0 \\ -8 \end{bmatrix} \end{array}$$

$$[b_{\text{REAL}}] \times [\text{CODE MATRIX}] = [R_{\text{REAL}}] = \text{"CHIPS OUT" ARRAY-REAL}$$

FIG. 20B

MAPPING FOR FALL-BACK MODE - LSB'S

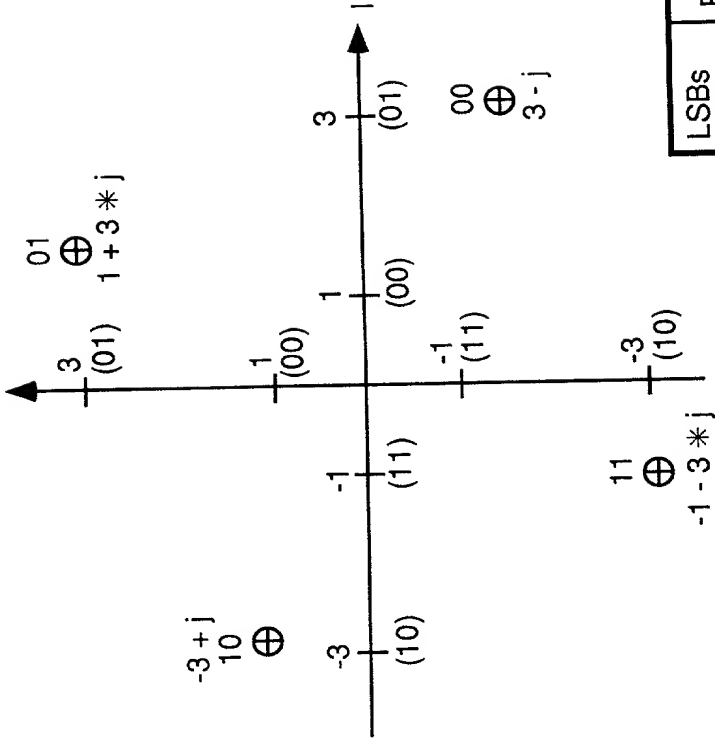


FIG. 21

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

LSB & MSB FALLBACK MODE MAPPINGS

FIG. 22

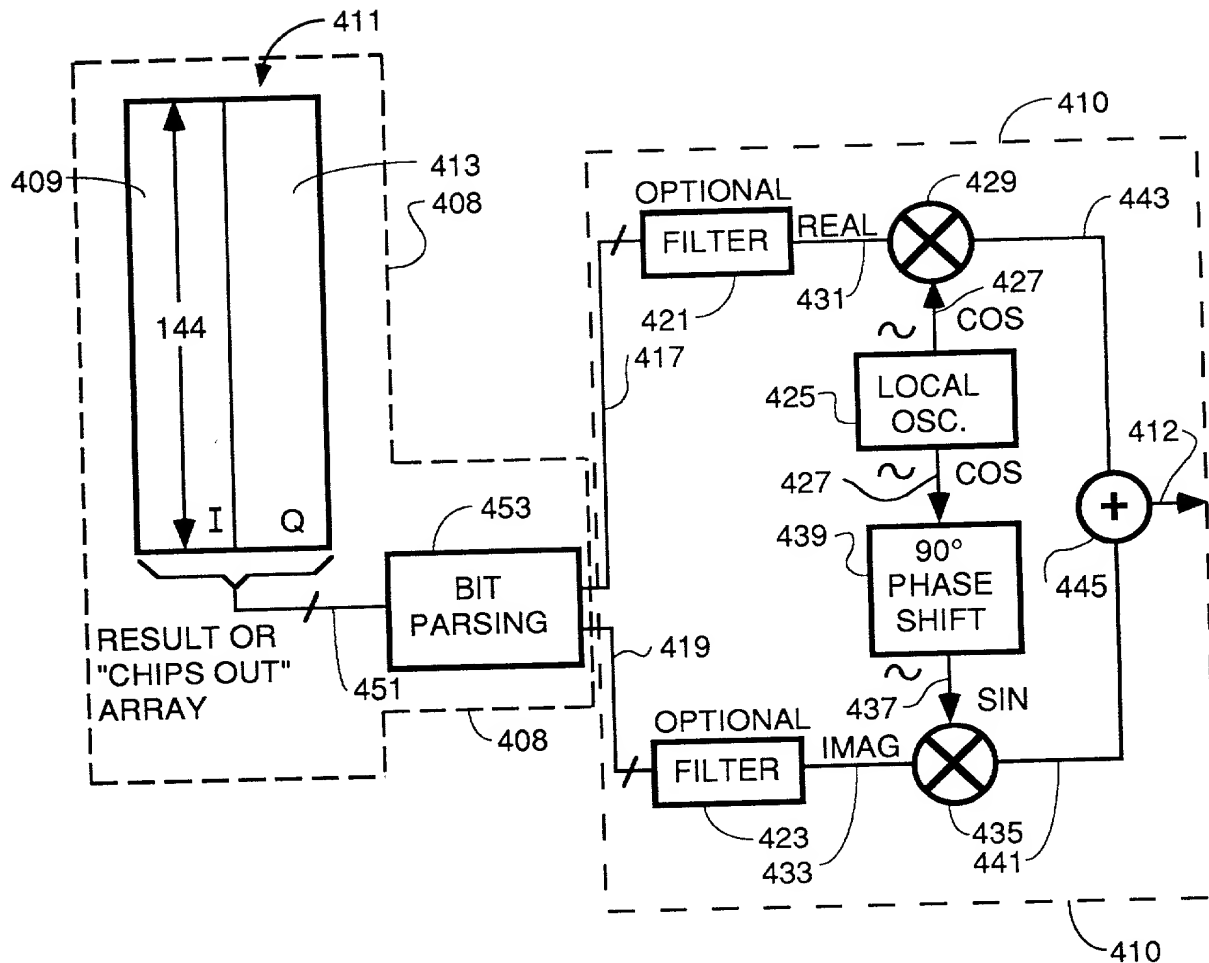


FIG. 23

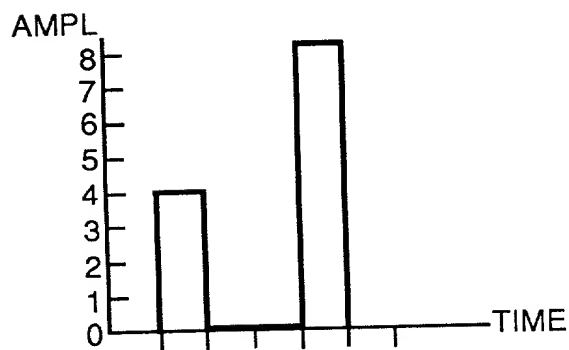


FIG. 24

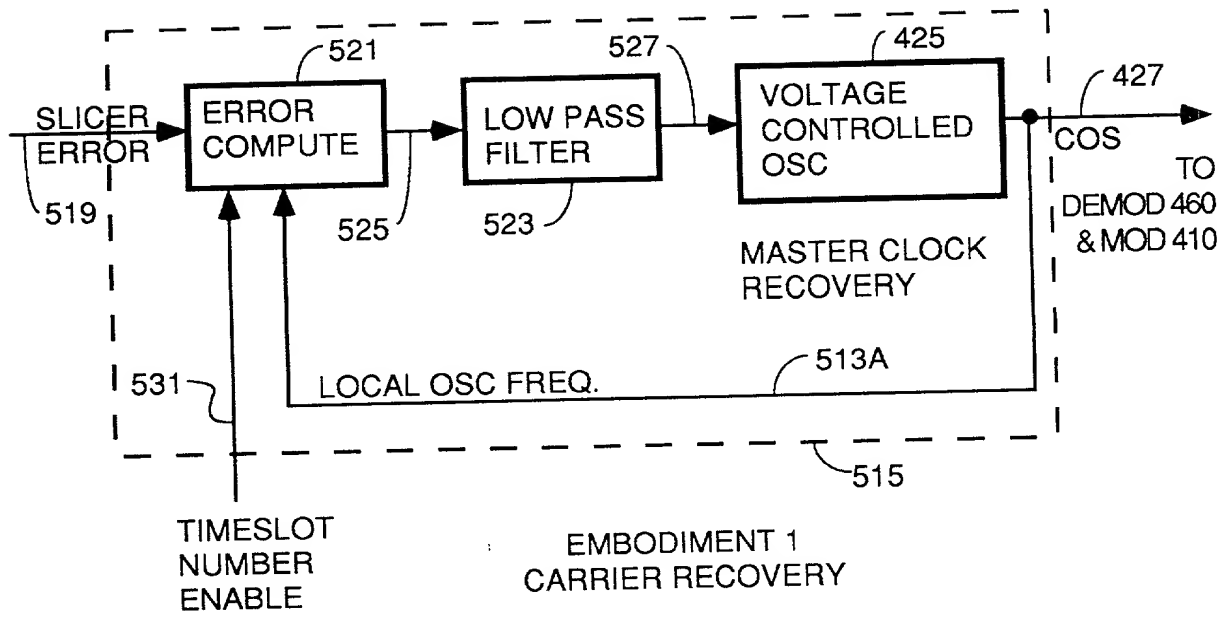


FIG. 25

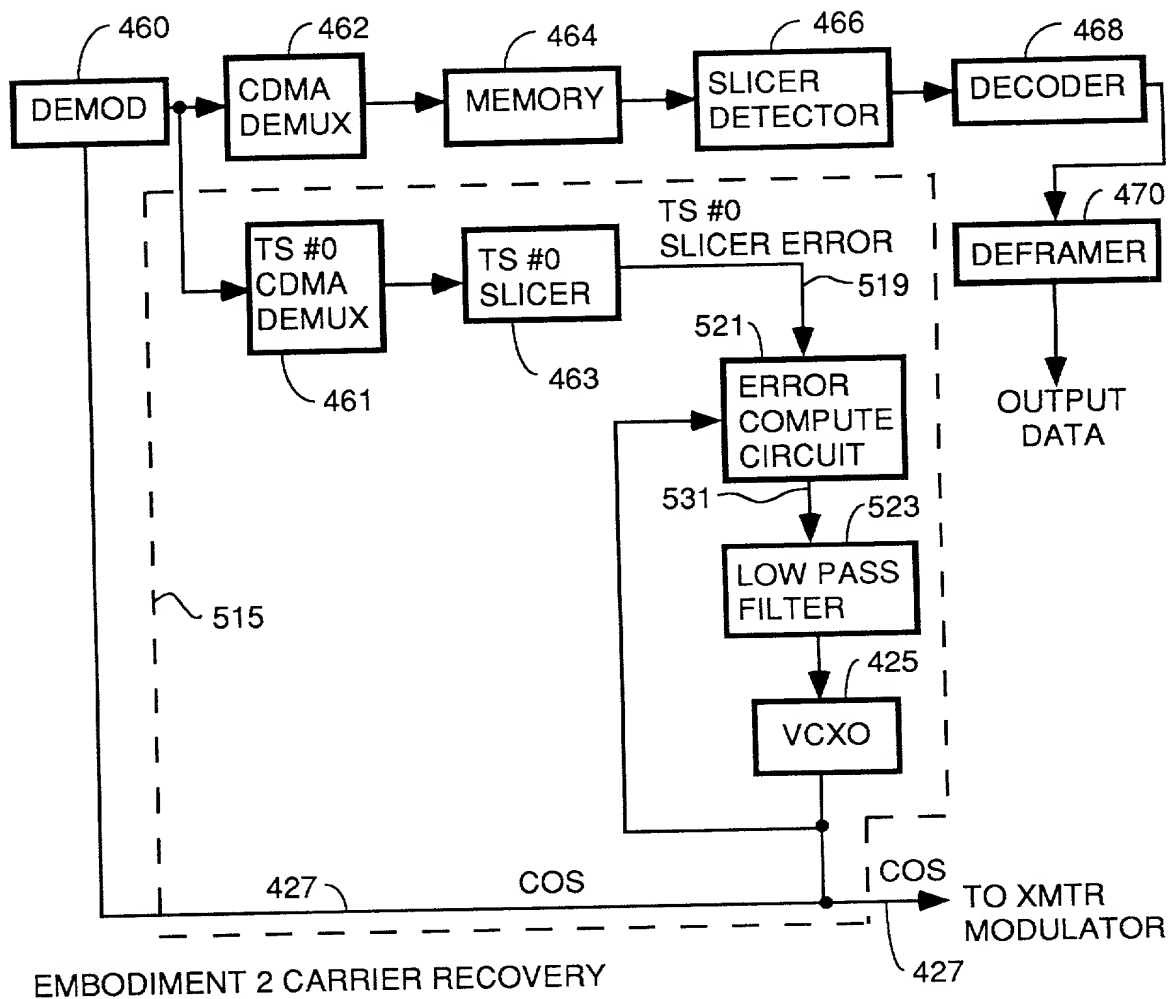


FIG. 26

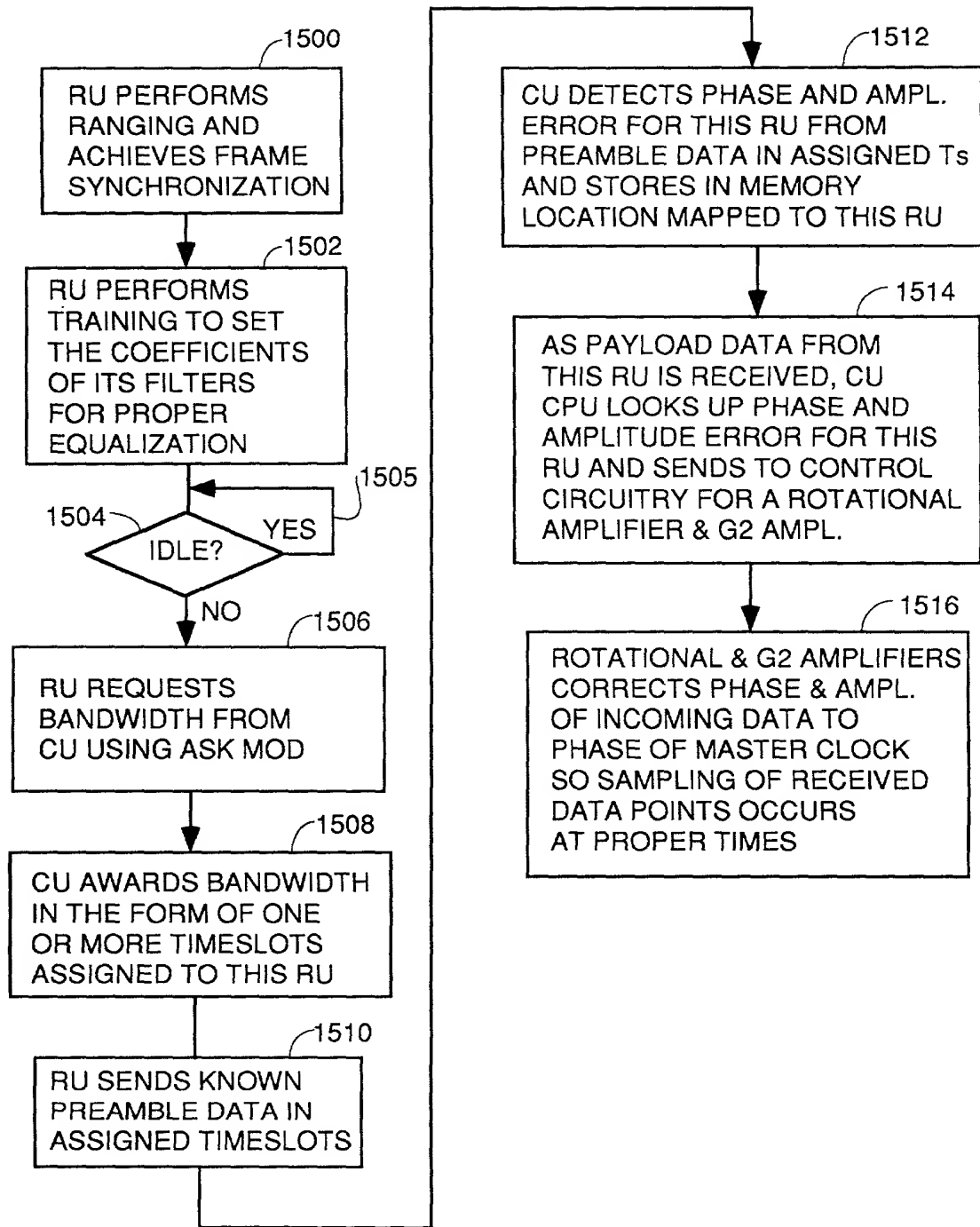
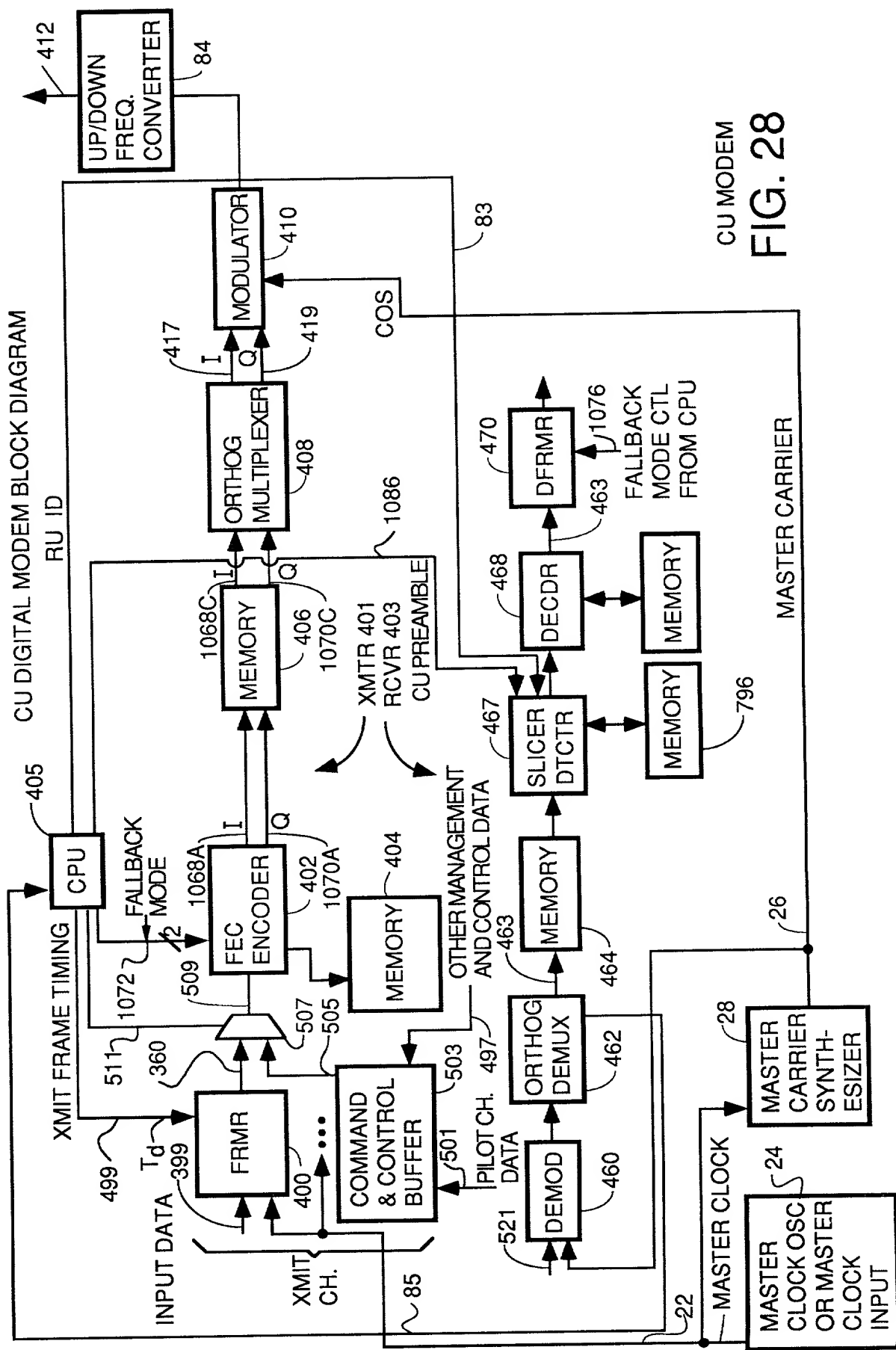


FIG. 27



CU MODEM
FIG. 28

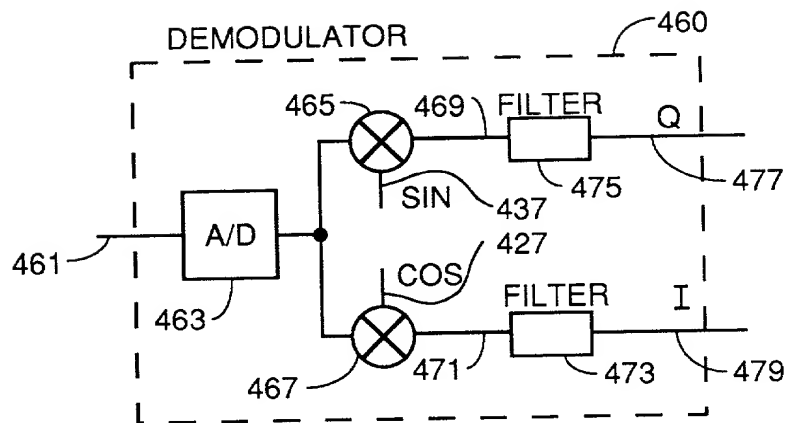


FIG. 29

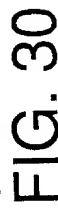
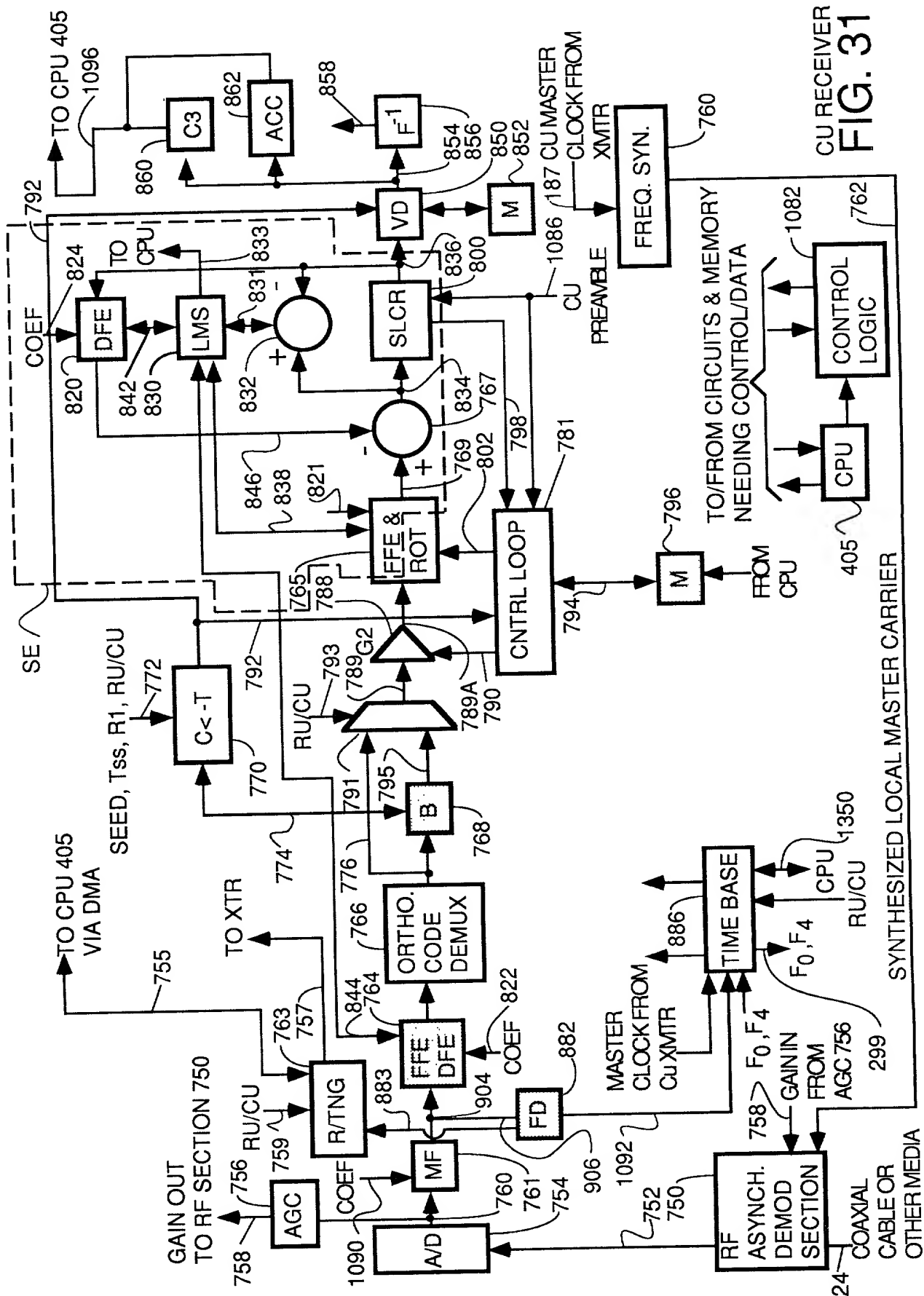
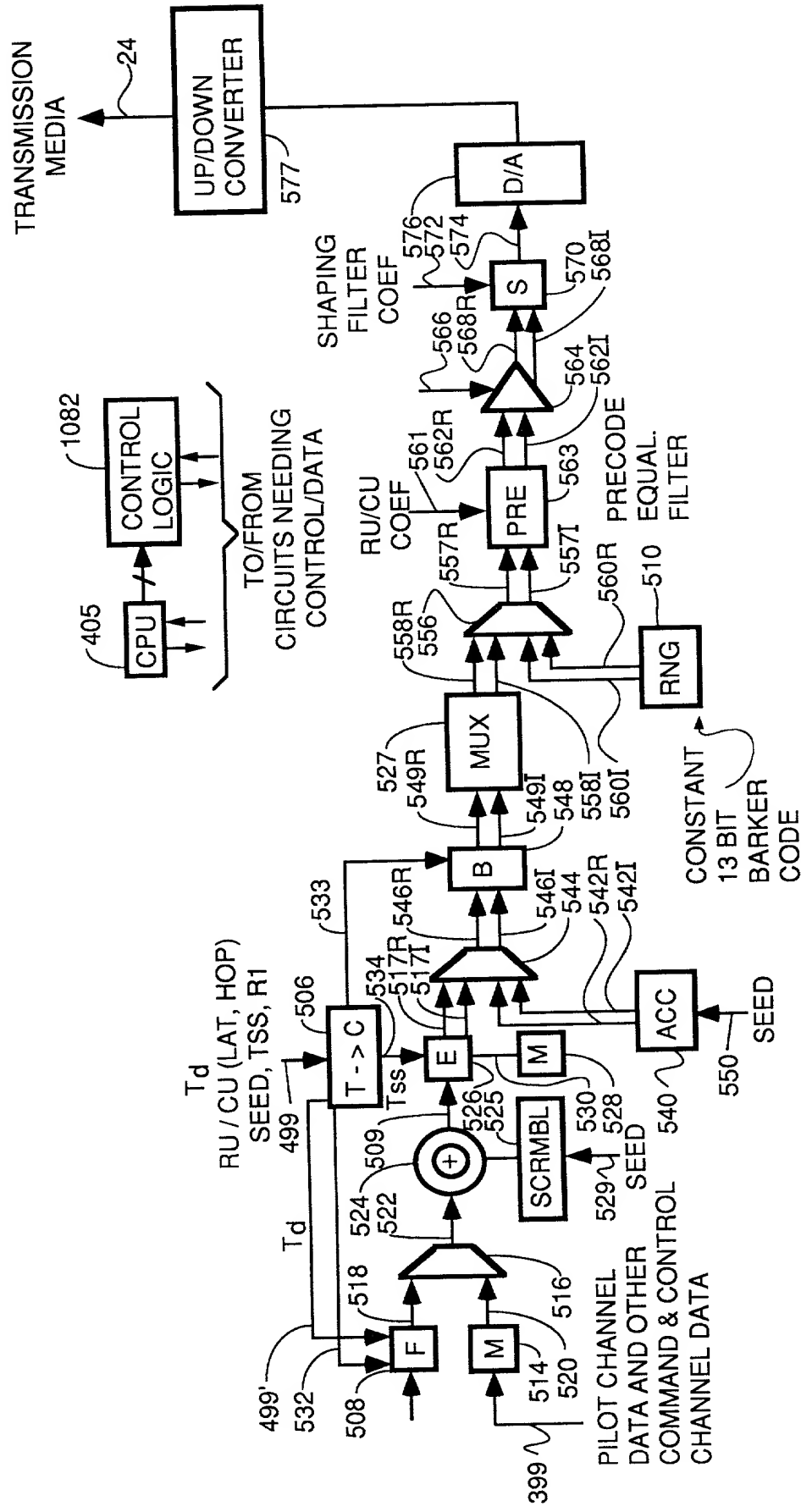


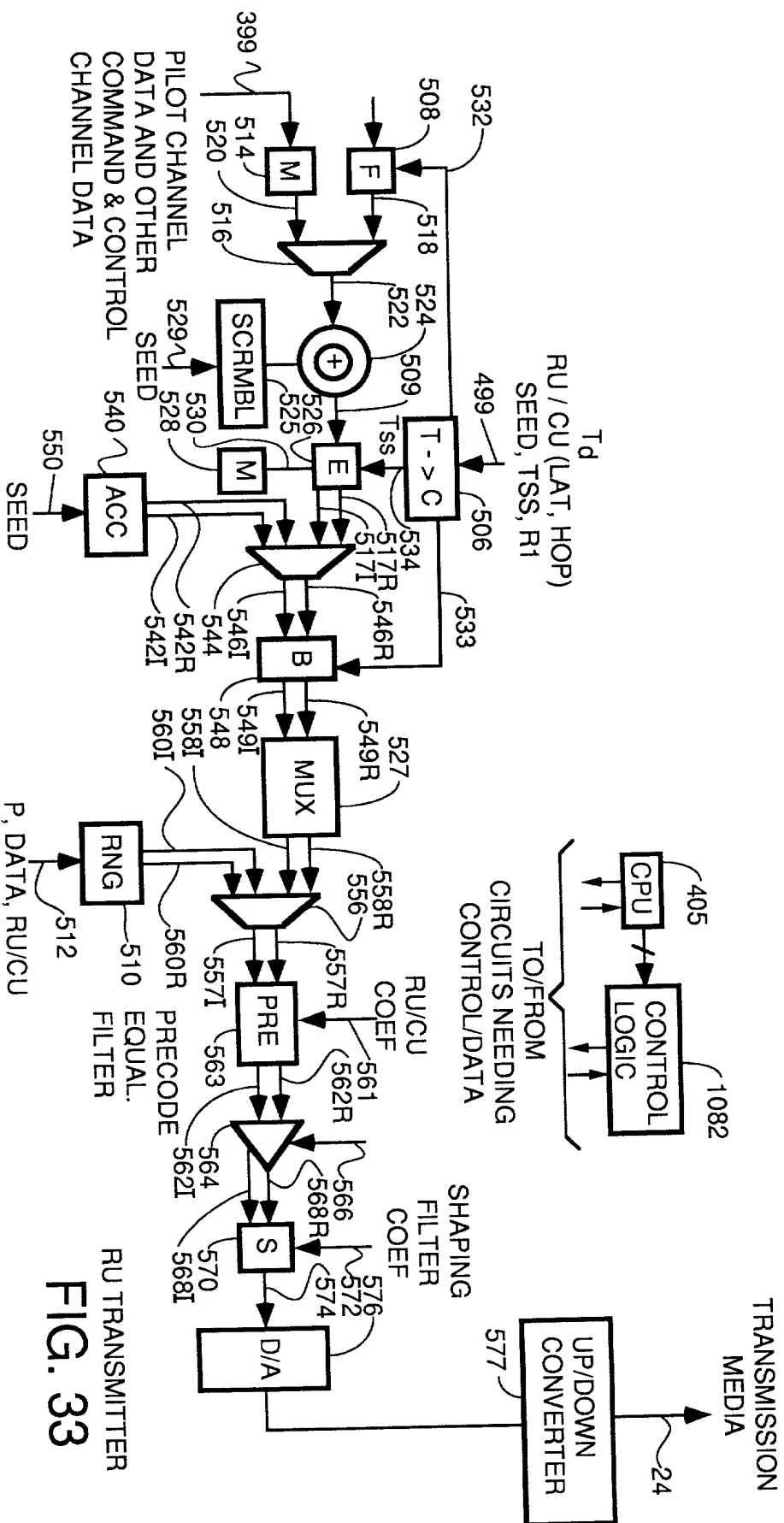
FIG. 30





CU TRANSMITTER

FIG. 32



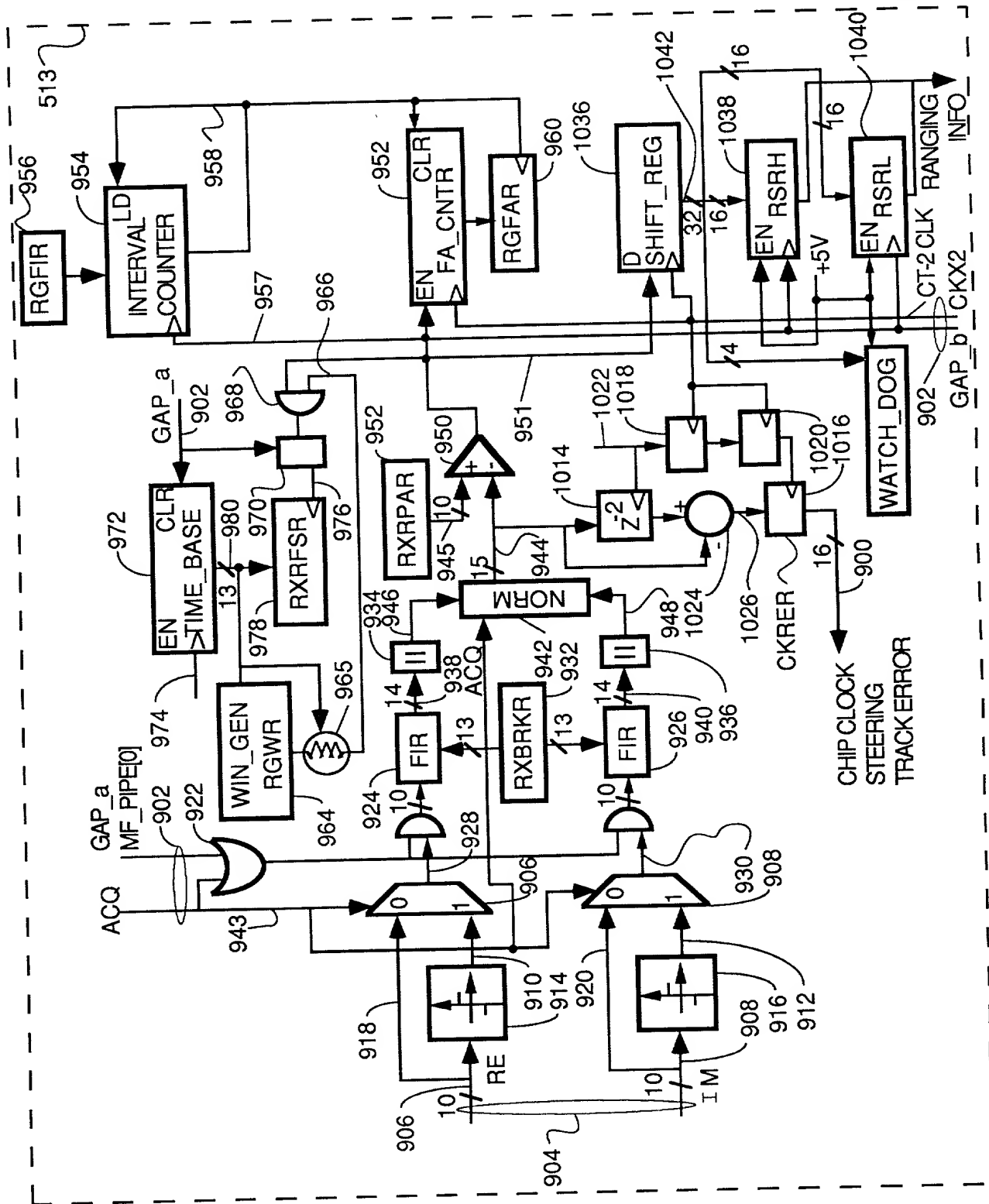


FIG. 34

FRAME
DETECTOR/
RANGING
DETECTOR

GAP ACQUISITION TIMING

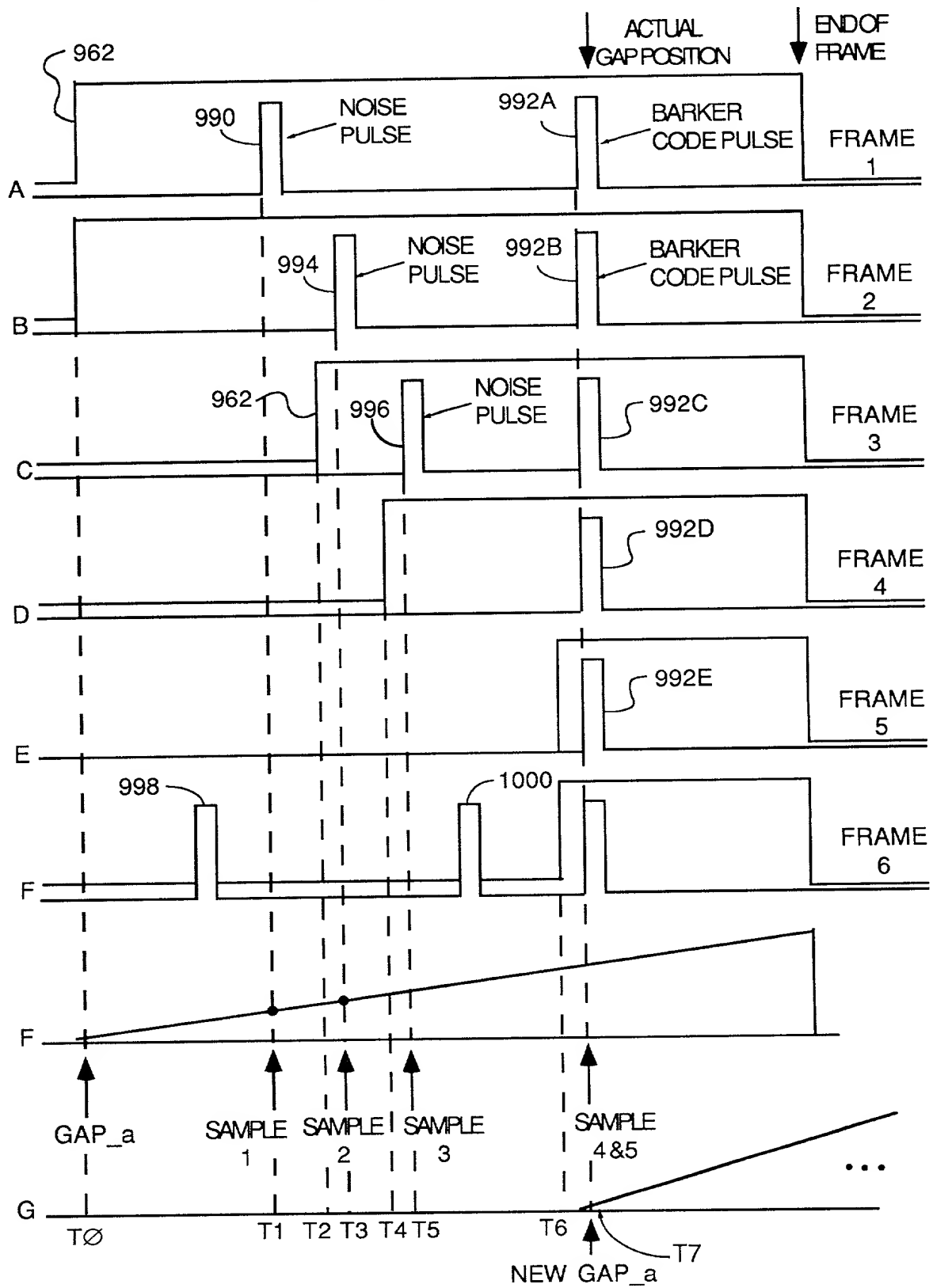


FIG. 35

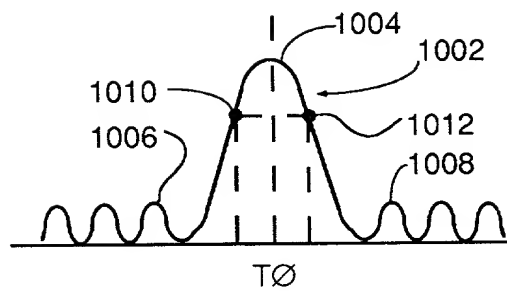


FIG. 36

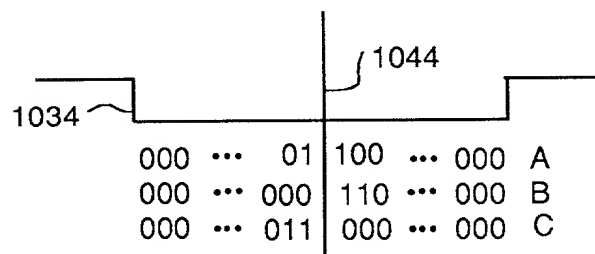


FIG. 37
FINE TUNING TO
CENTER BARKER CODE

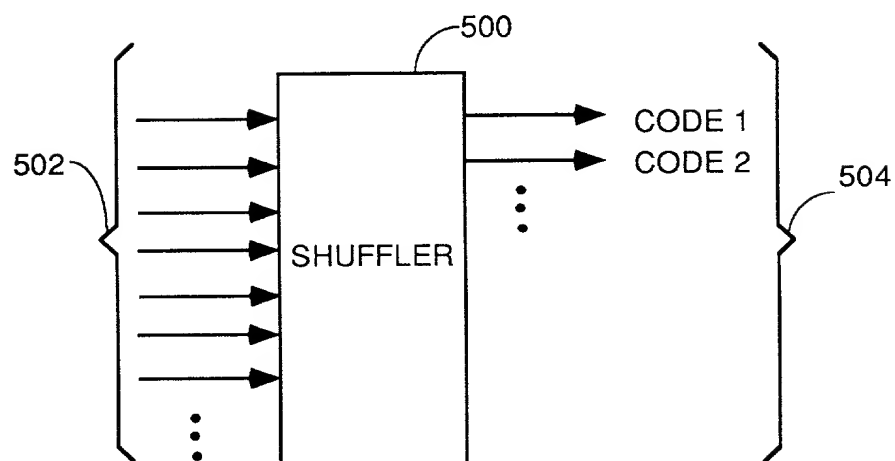


FIG. 38

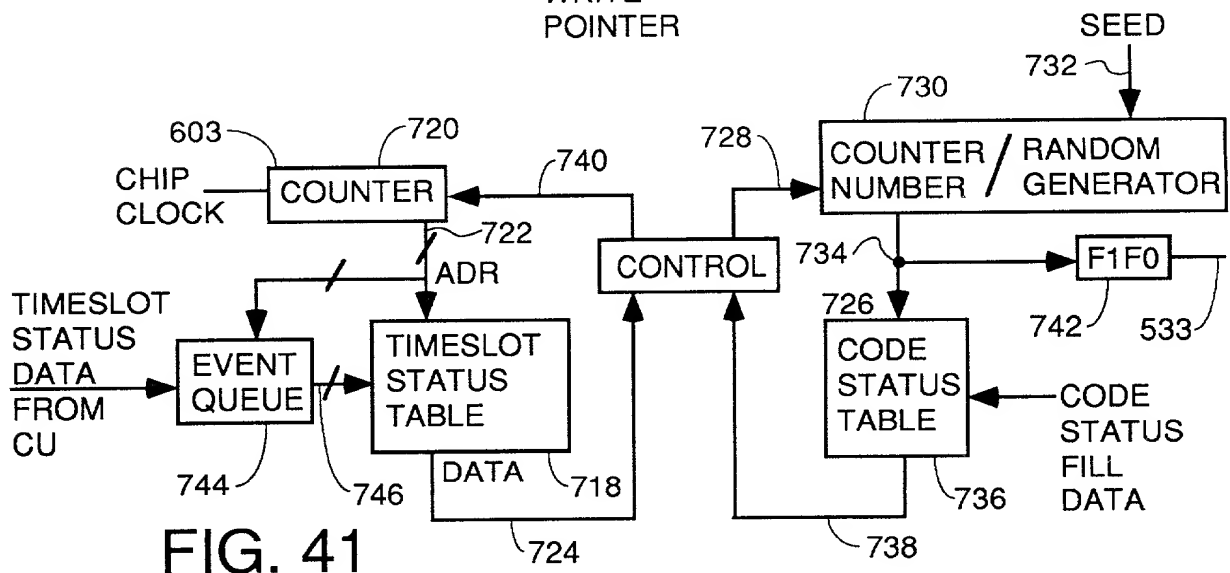
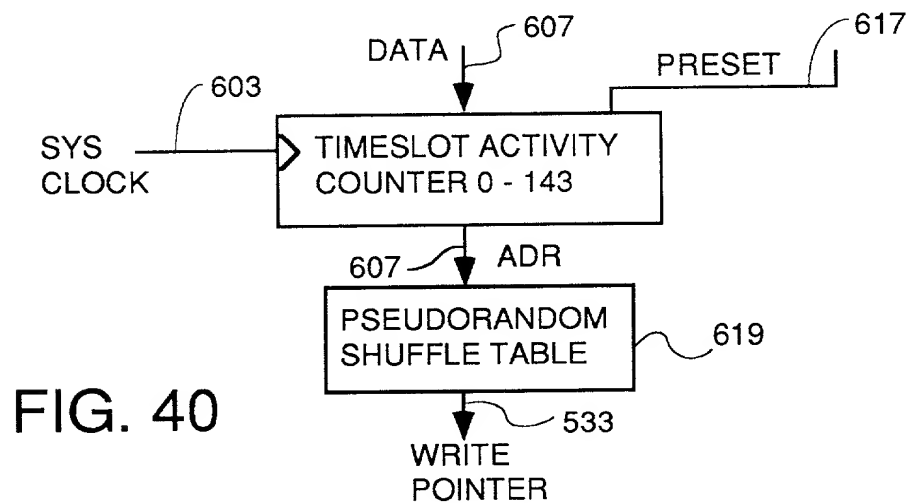
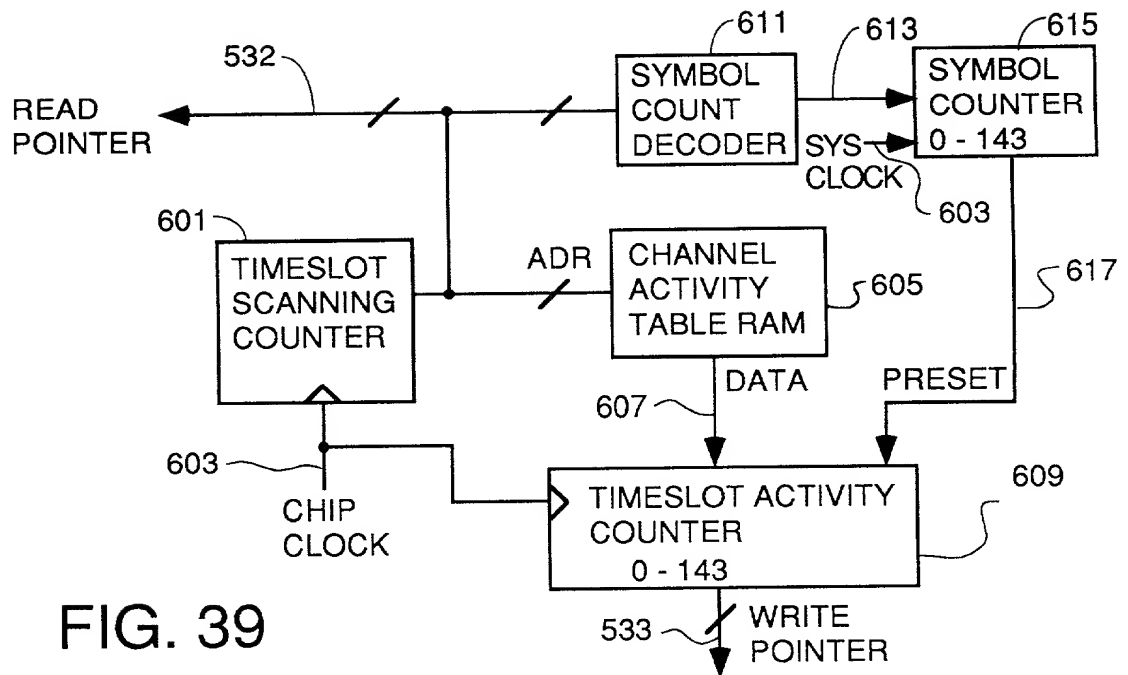


FIG. 42

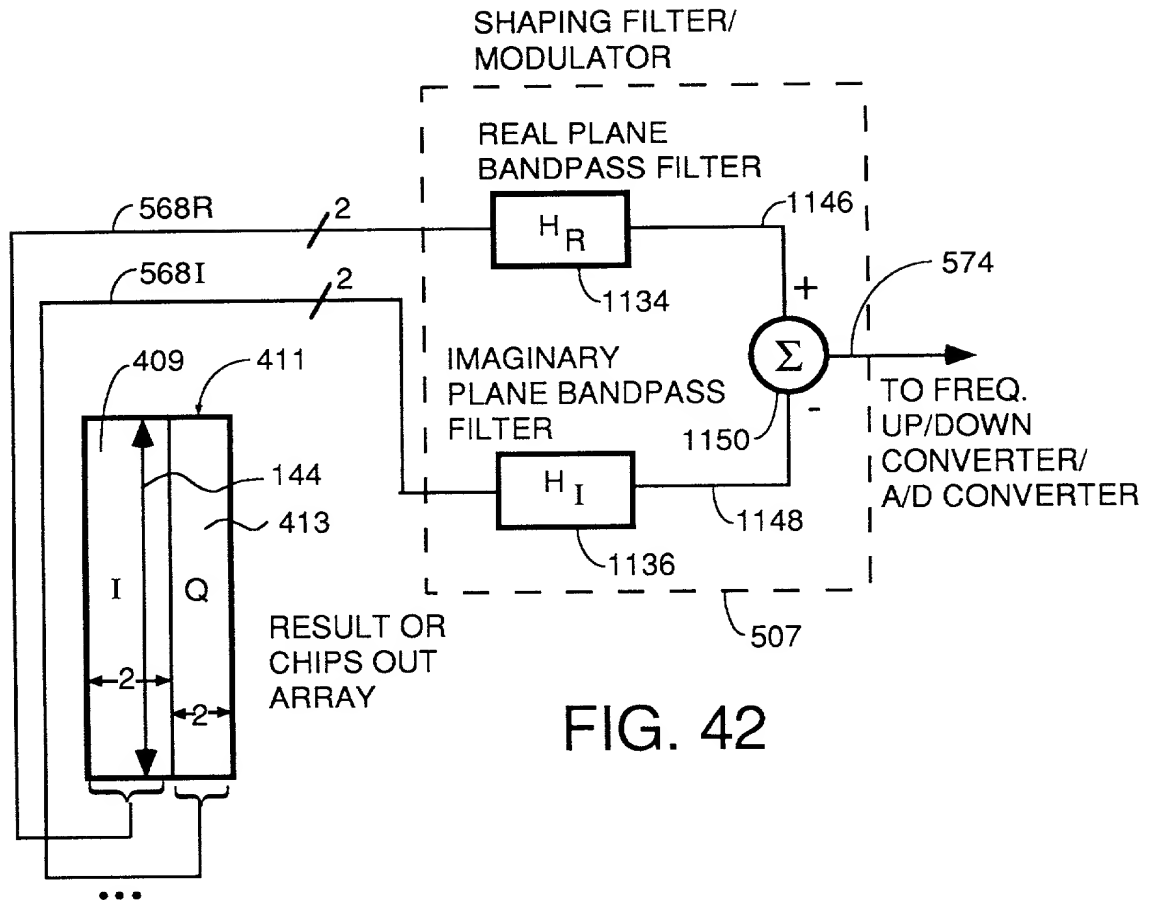


FIG. 42

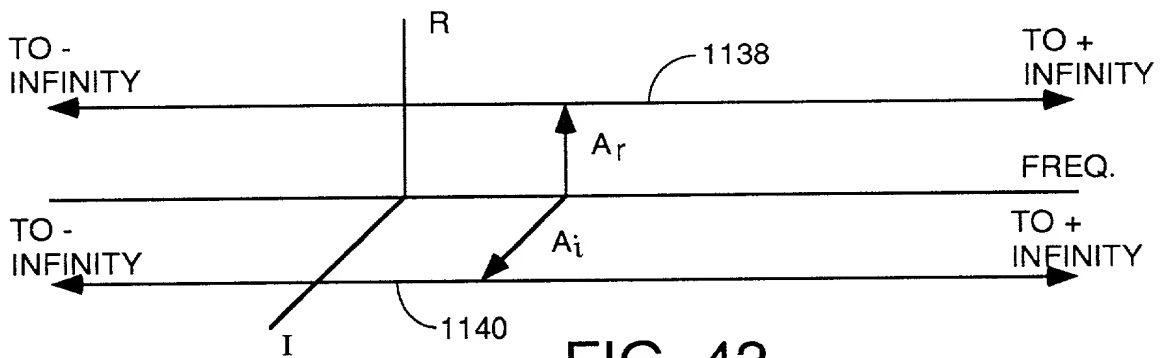


FIG. 43

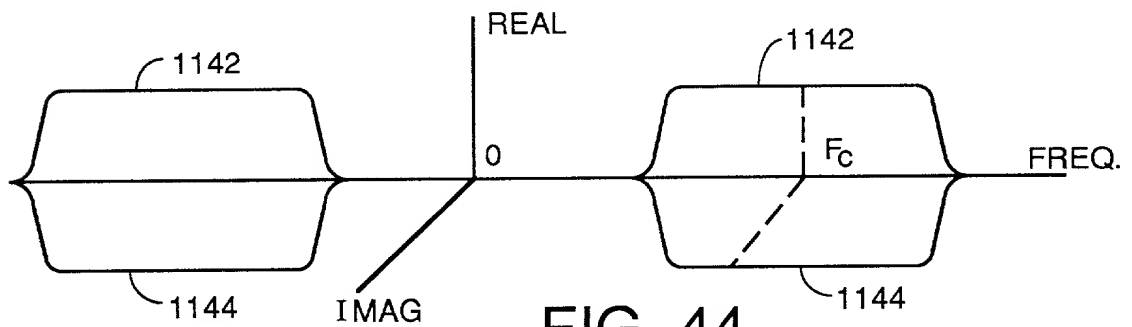
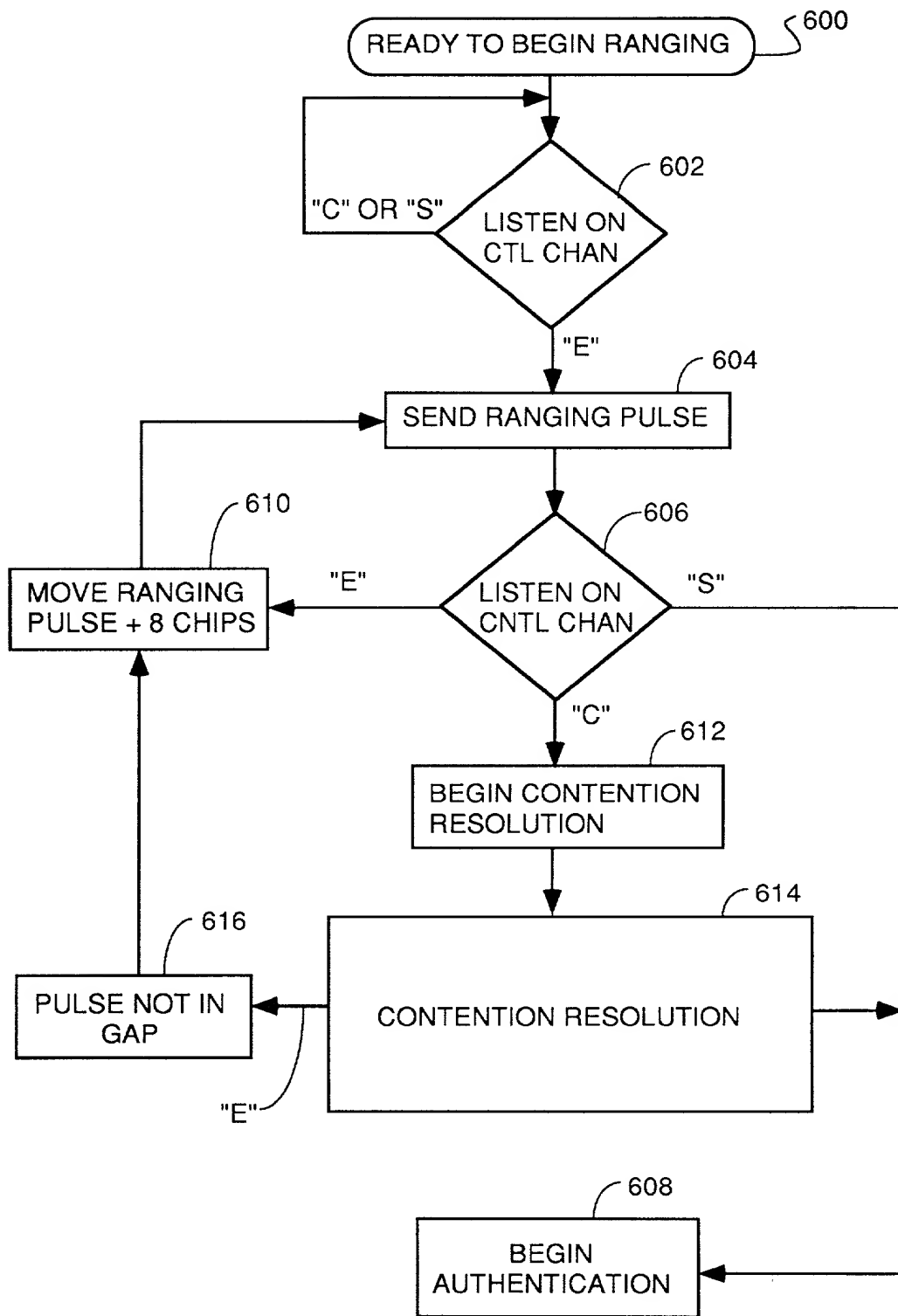
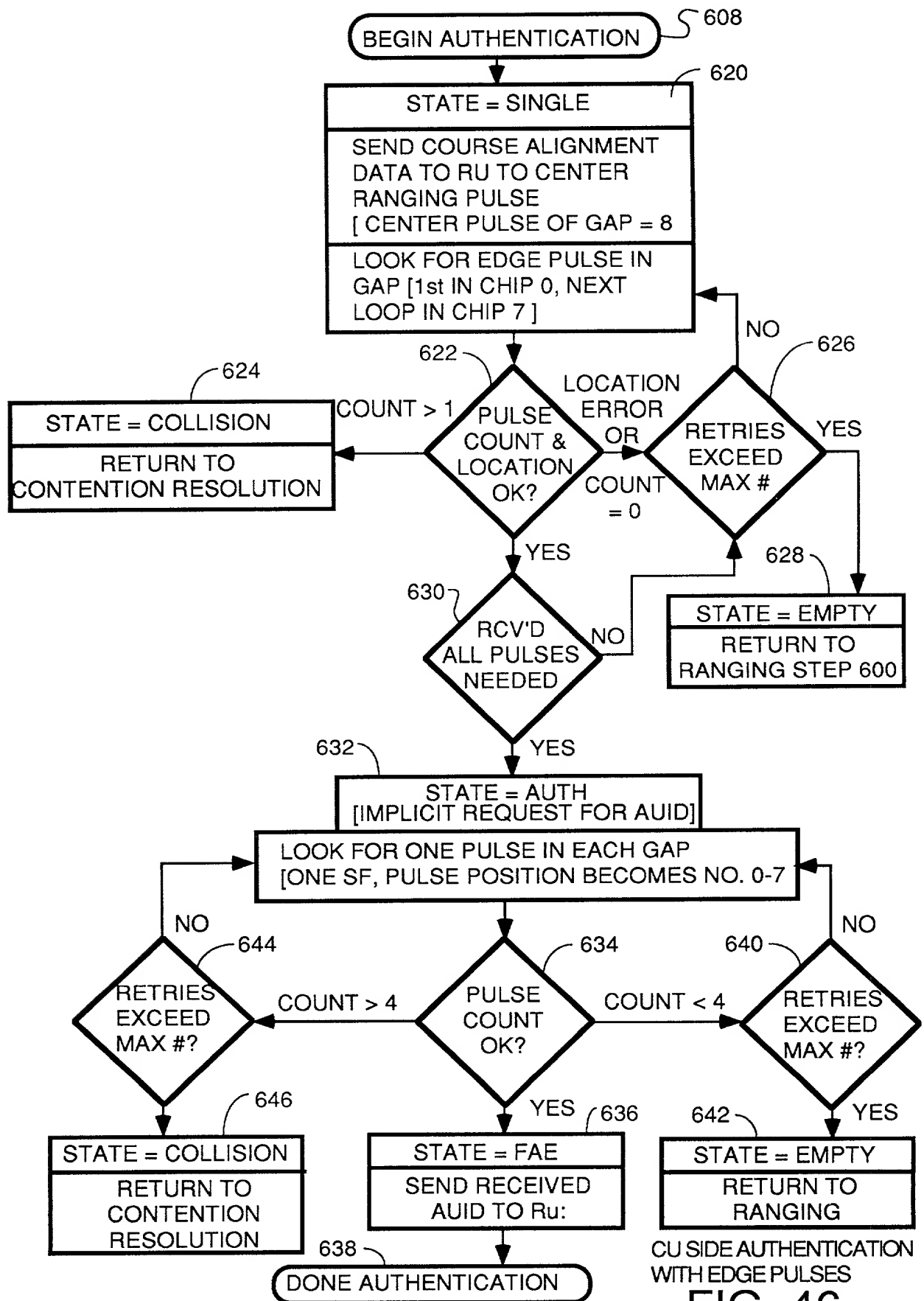
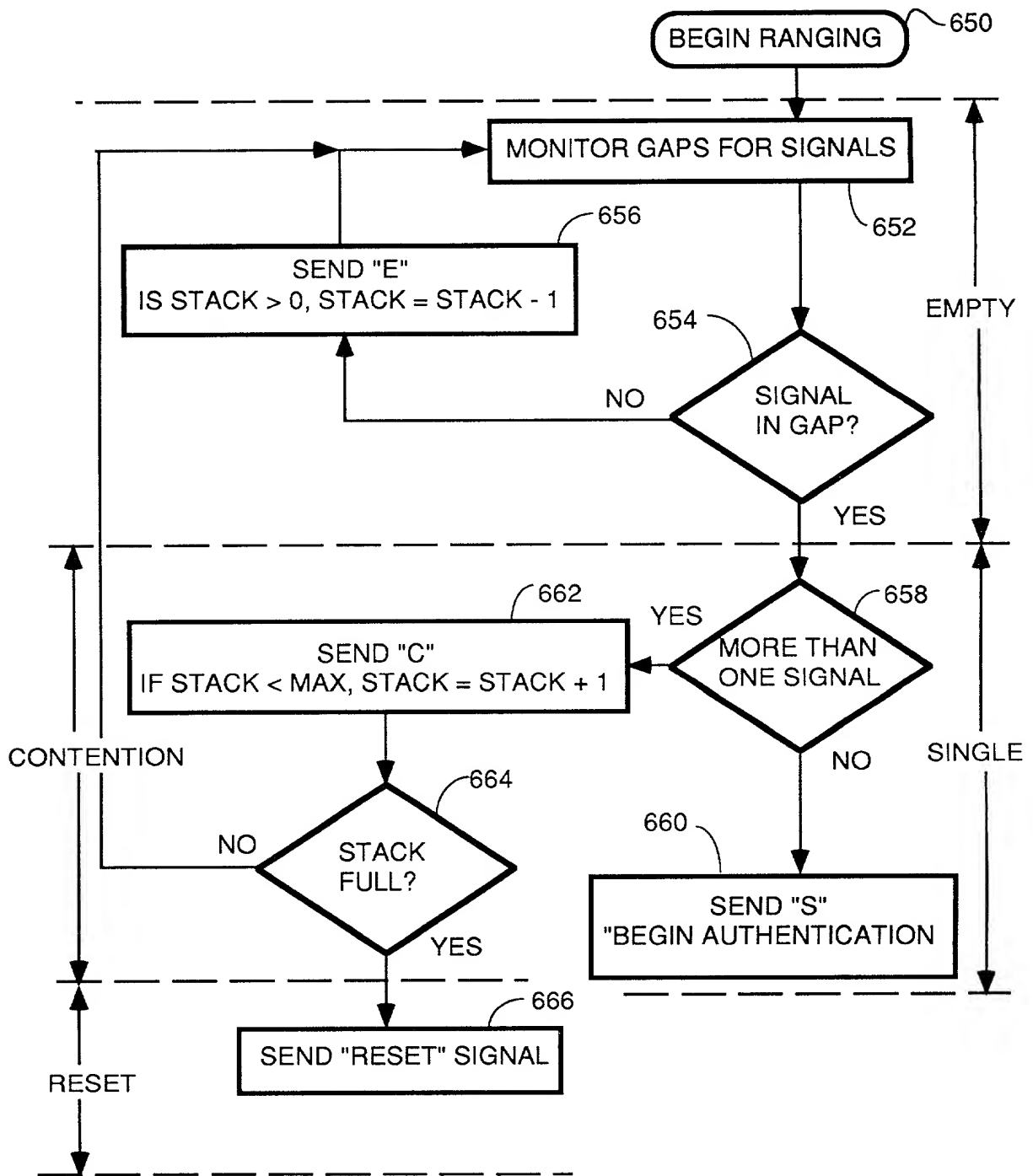


FIG. 44



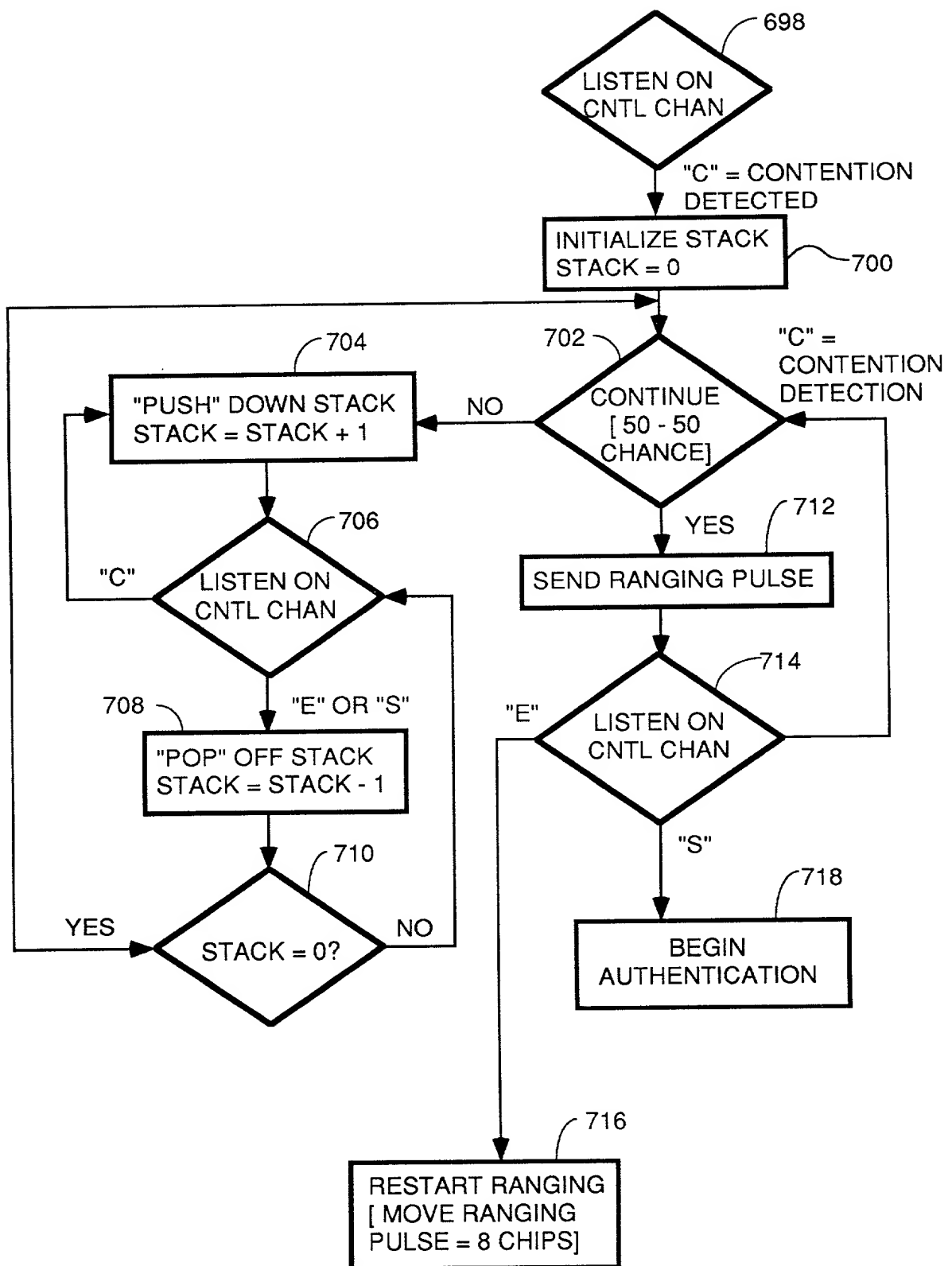
RU RANGING
FIG. 45





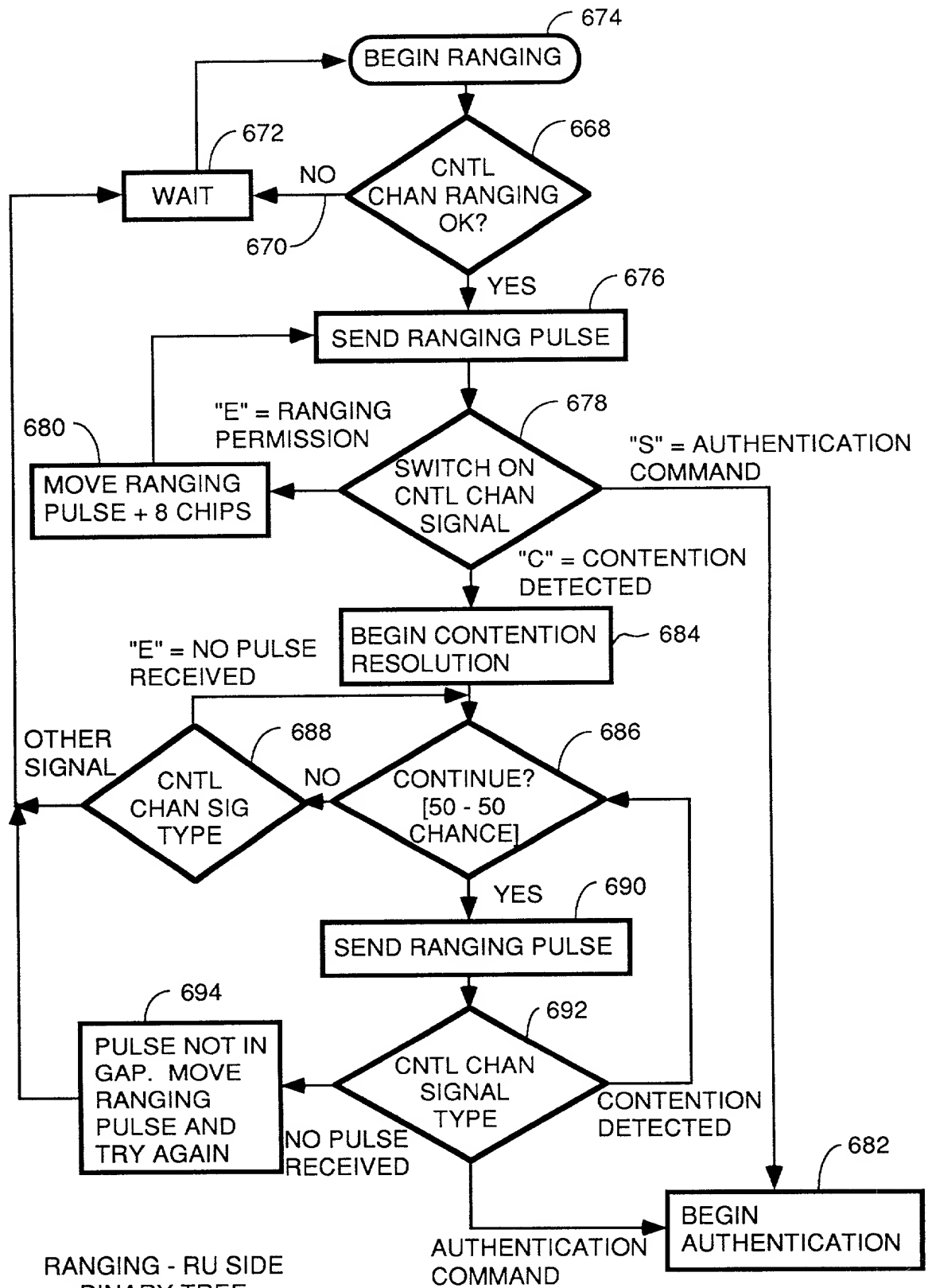
CU RANGING AND CONTENTION RESOLUTION

FIG. 47



CONTENTION RESOLUTION - RU
USING BINARY STACK

FIG. 48



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 49

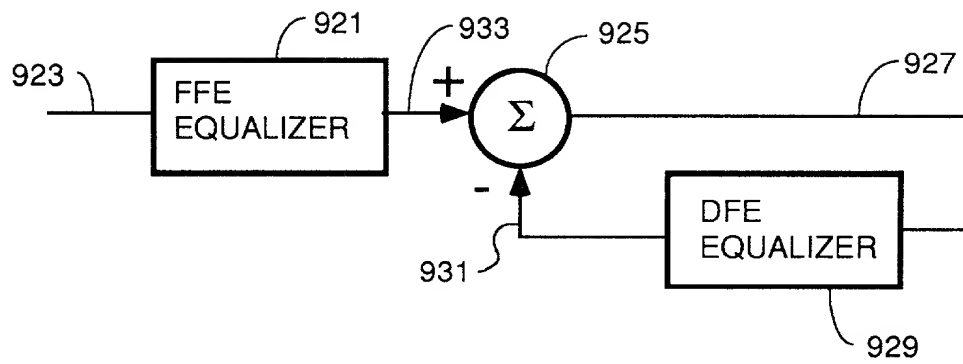


FIG. 50

[illegible]

PRECHANNEL EQUALIZATION
TRAINING ALGORITHM

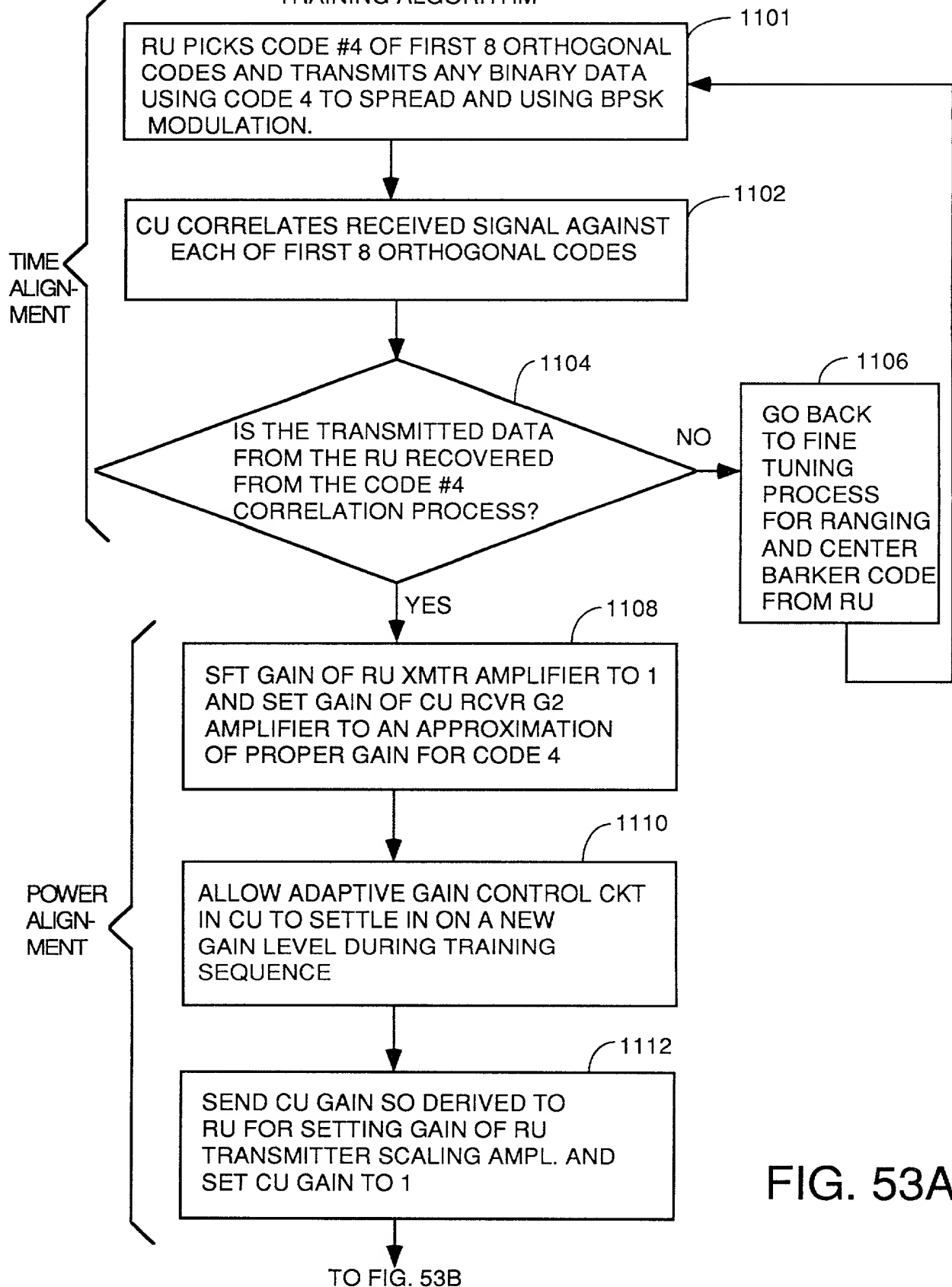


FIG. 53A

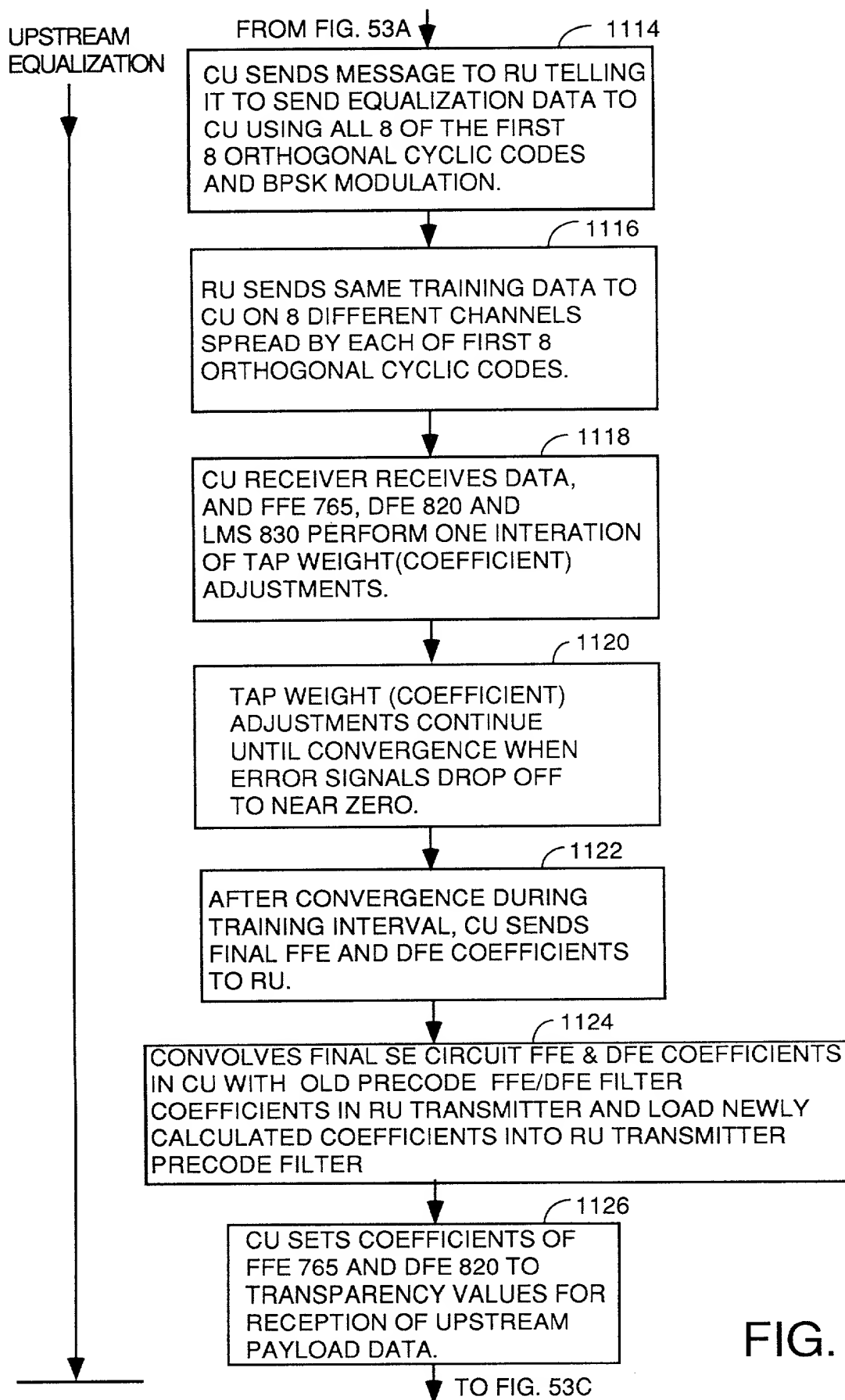


FIG. 53B

DOWNSTREAM
EQUALIZATION

FROM FIG. 53B

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AND DFE FILTERS OF CE CIRCUIT 764 AND LOADS THE NEWLY CALCULATED TAP WEIGHTS INTO THE FFE AND DFE FILTERS OF THE CE CIRCUIT; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

FIG. 53C

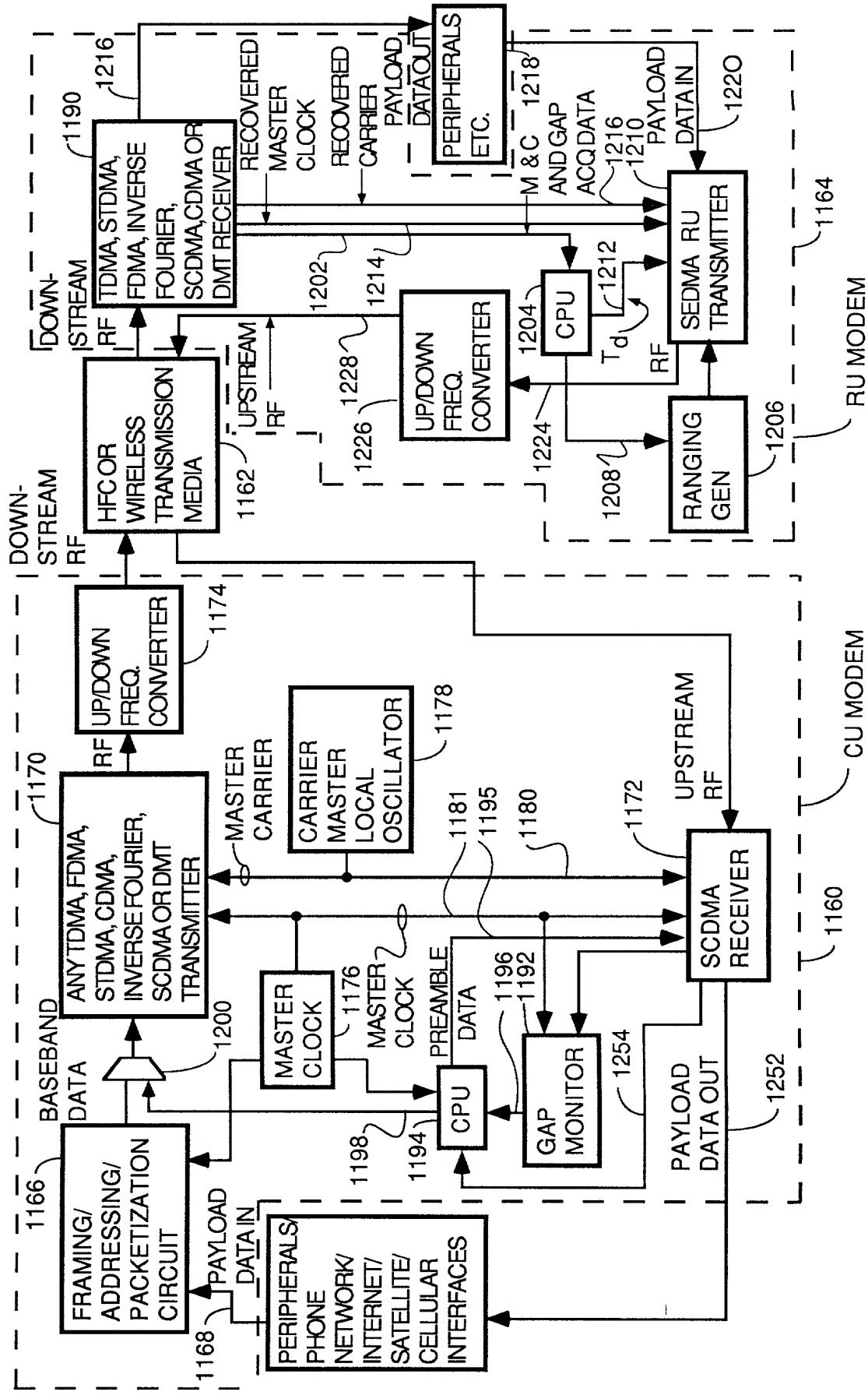
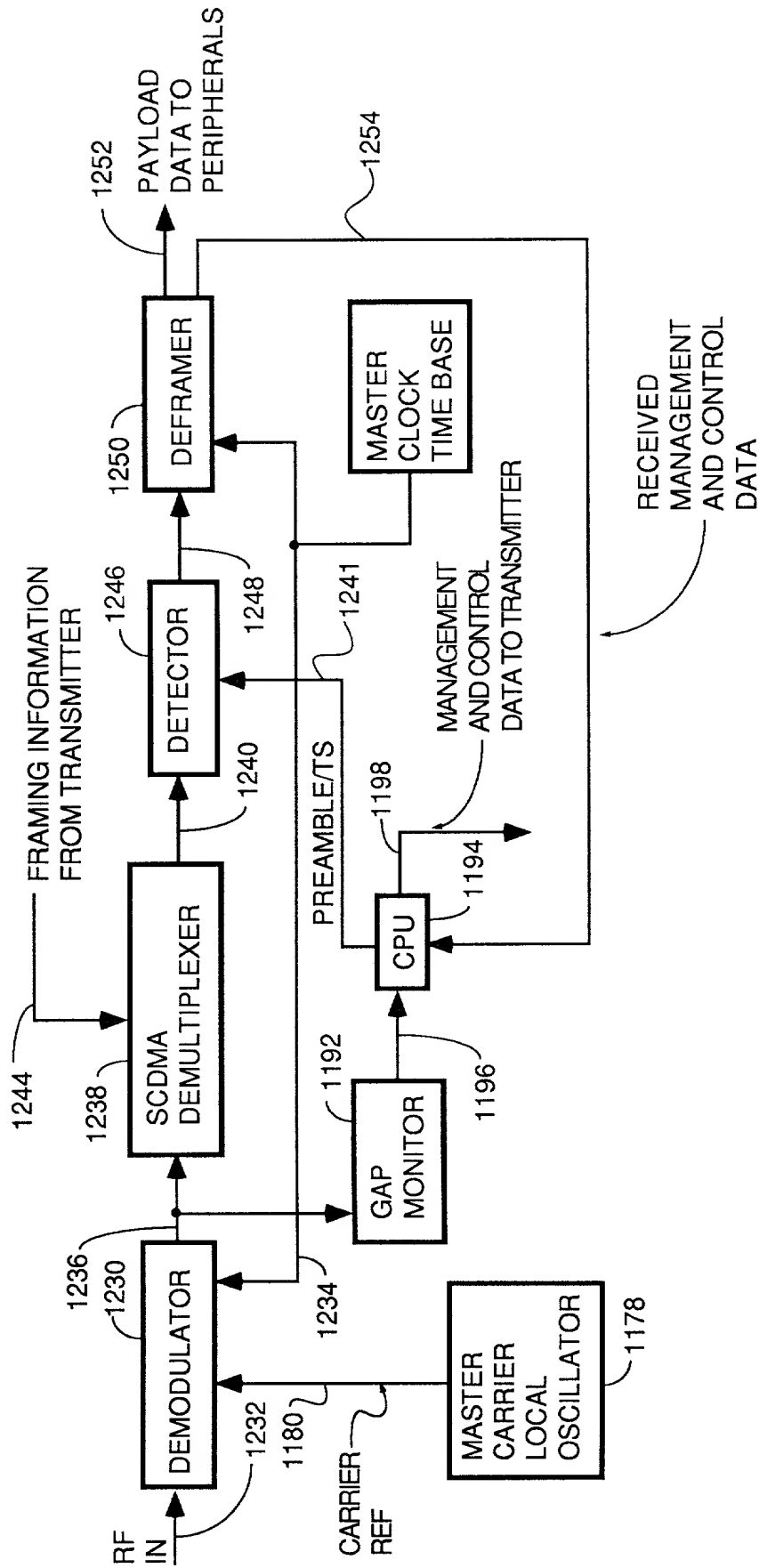


FIG. 54



SIMPLE CU SPREAD SPECTRUM RECEIVER

FIG. 55

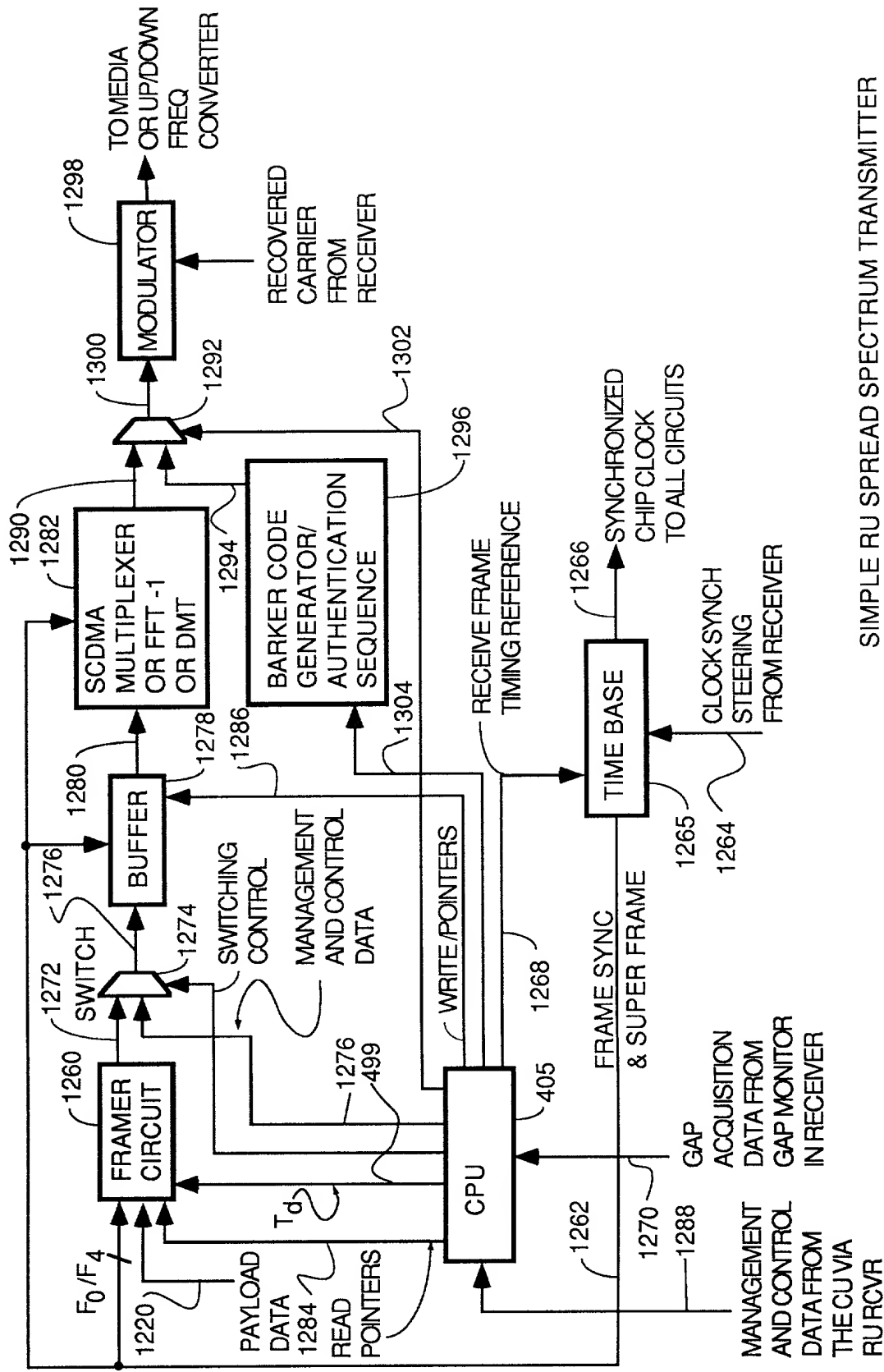
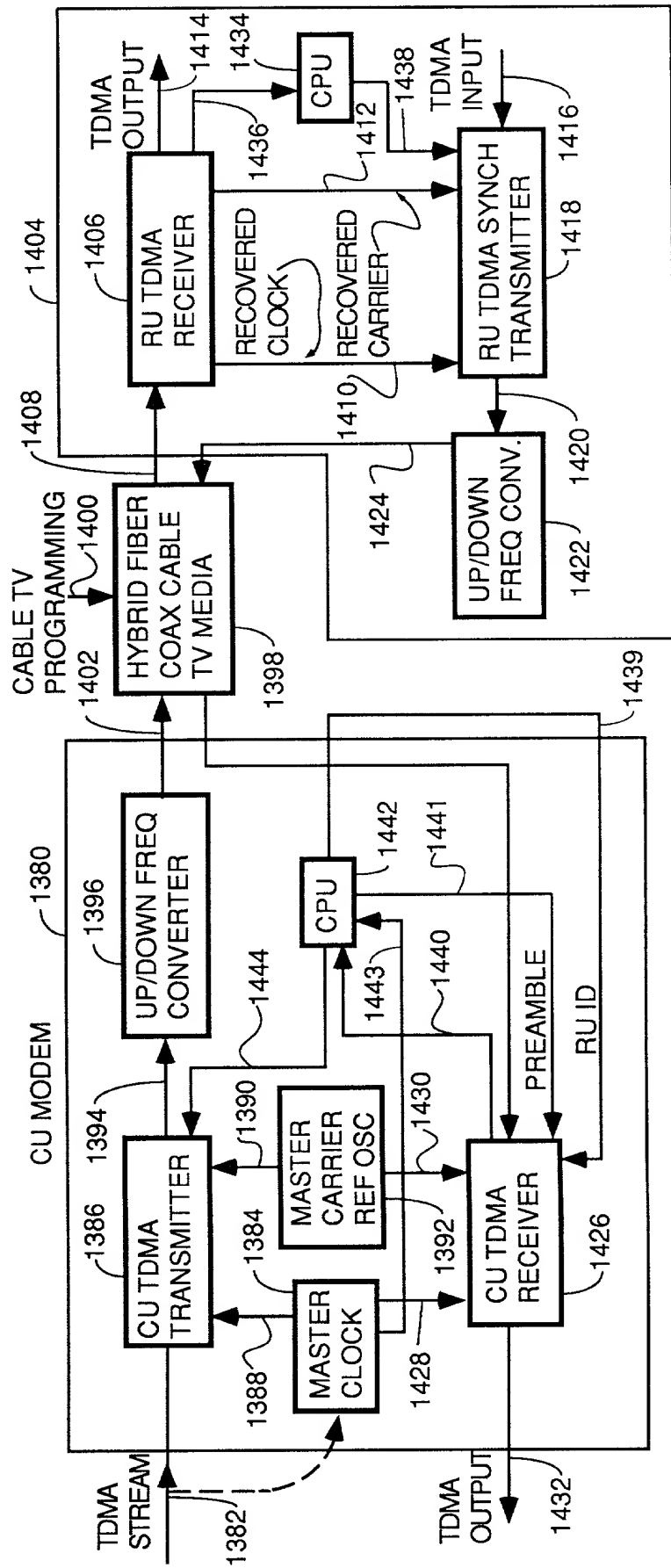


FIG. 56

SIMPLE RU SPREAD SPECTRUM TRANSMITTER



SYNCHRONOUS TDMA SYSTEM

FIG. 57

FIG. 40

OFFSET (CHIPS)	1B ASIC		2A ASIC	
	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

TRAINING ALGORITHM

SE FUNCTION

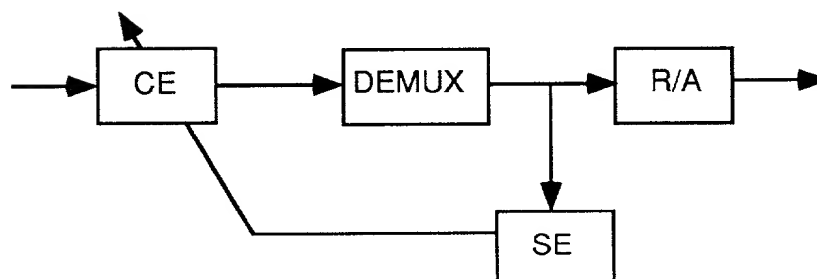
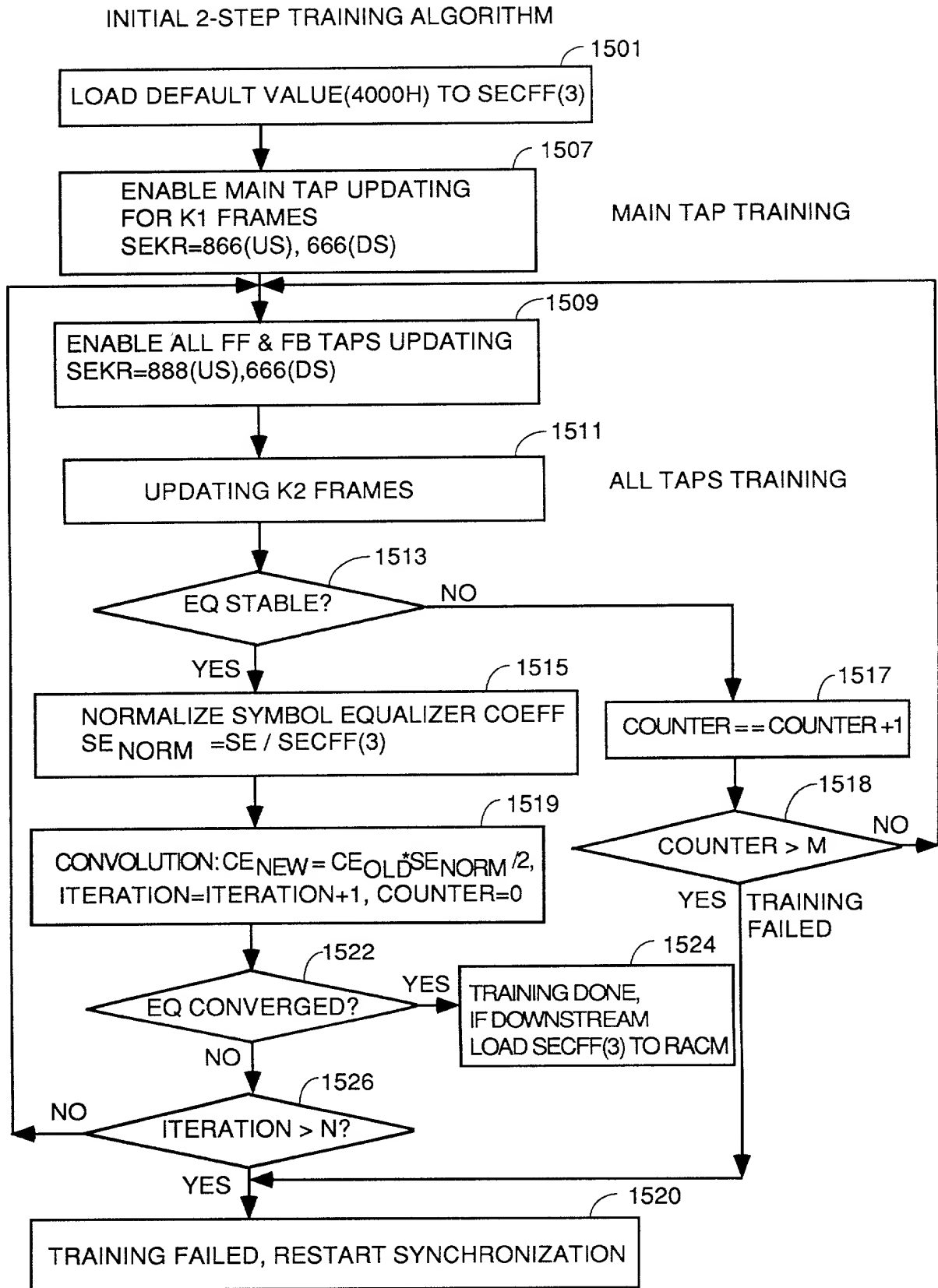


FIG. 59



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

EQ STABILITY CHECK

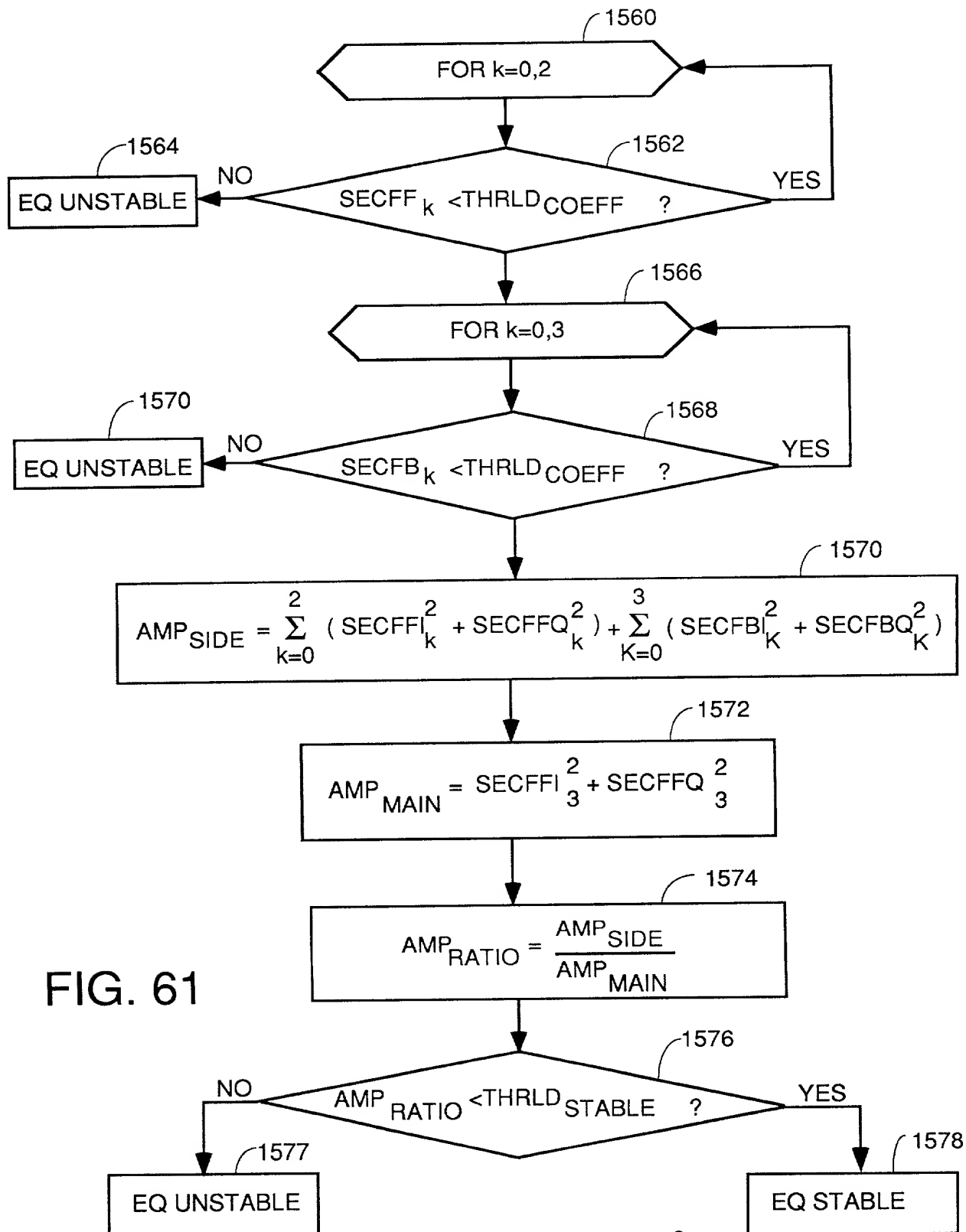


FIG. 61

NOTE: THRLD_{COEFF} = 7F00H

THRLD_{STABLE} = 10⁻³

PERIODIC 2-STEP TRAINING ALGORITHM

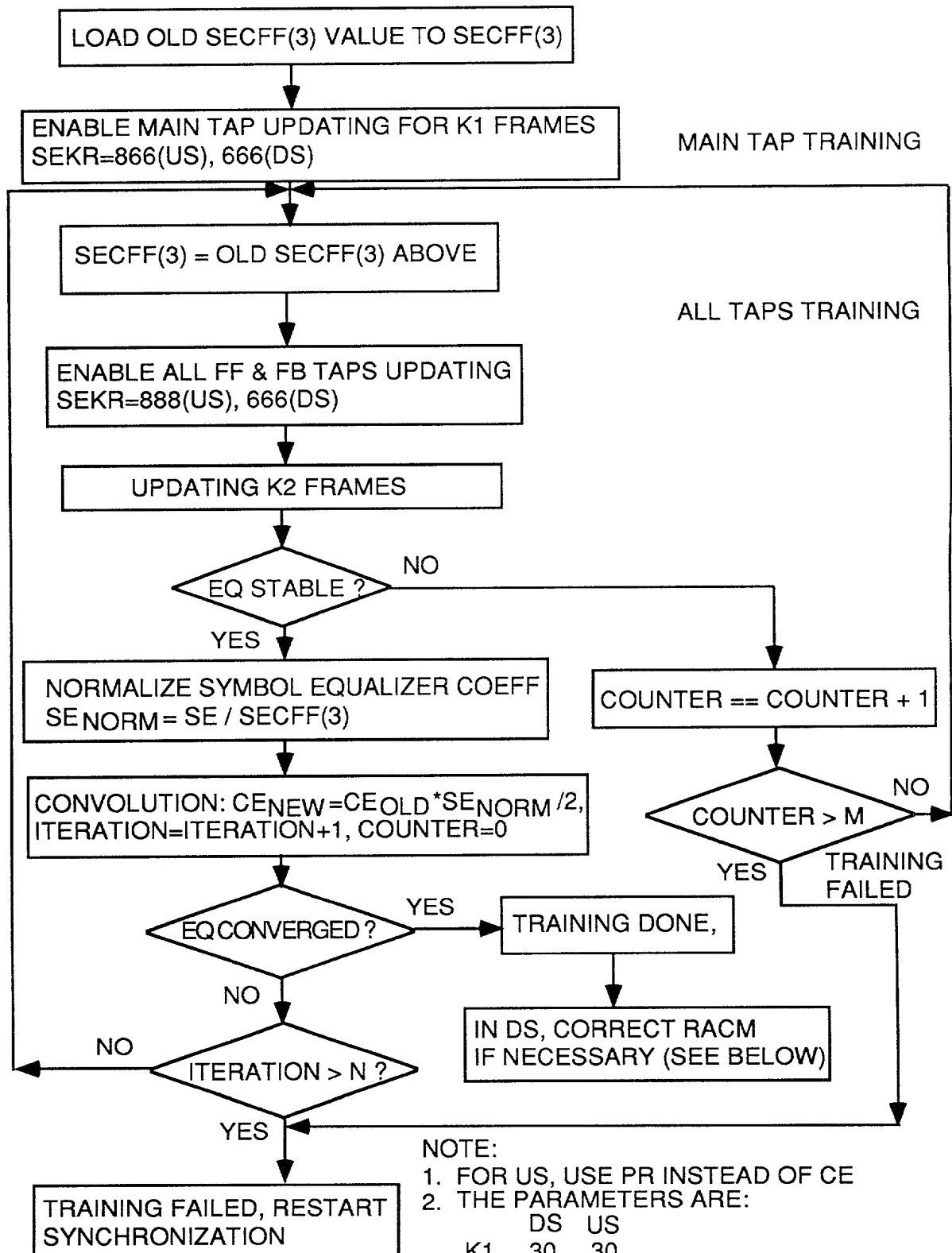
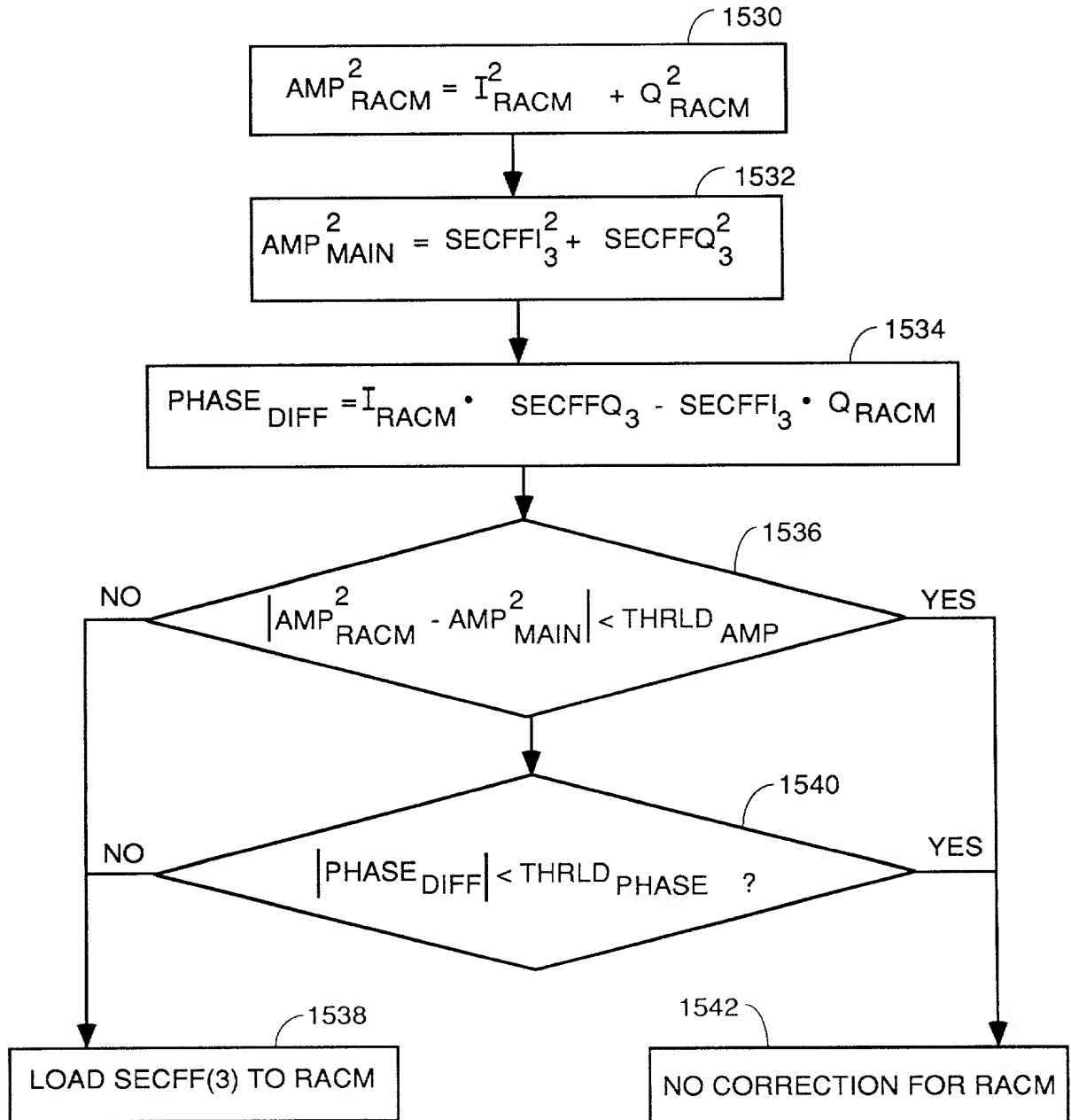


FIG. 62

RACM CORRECTION

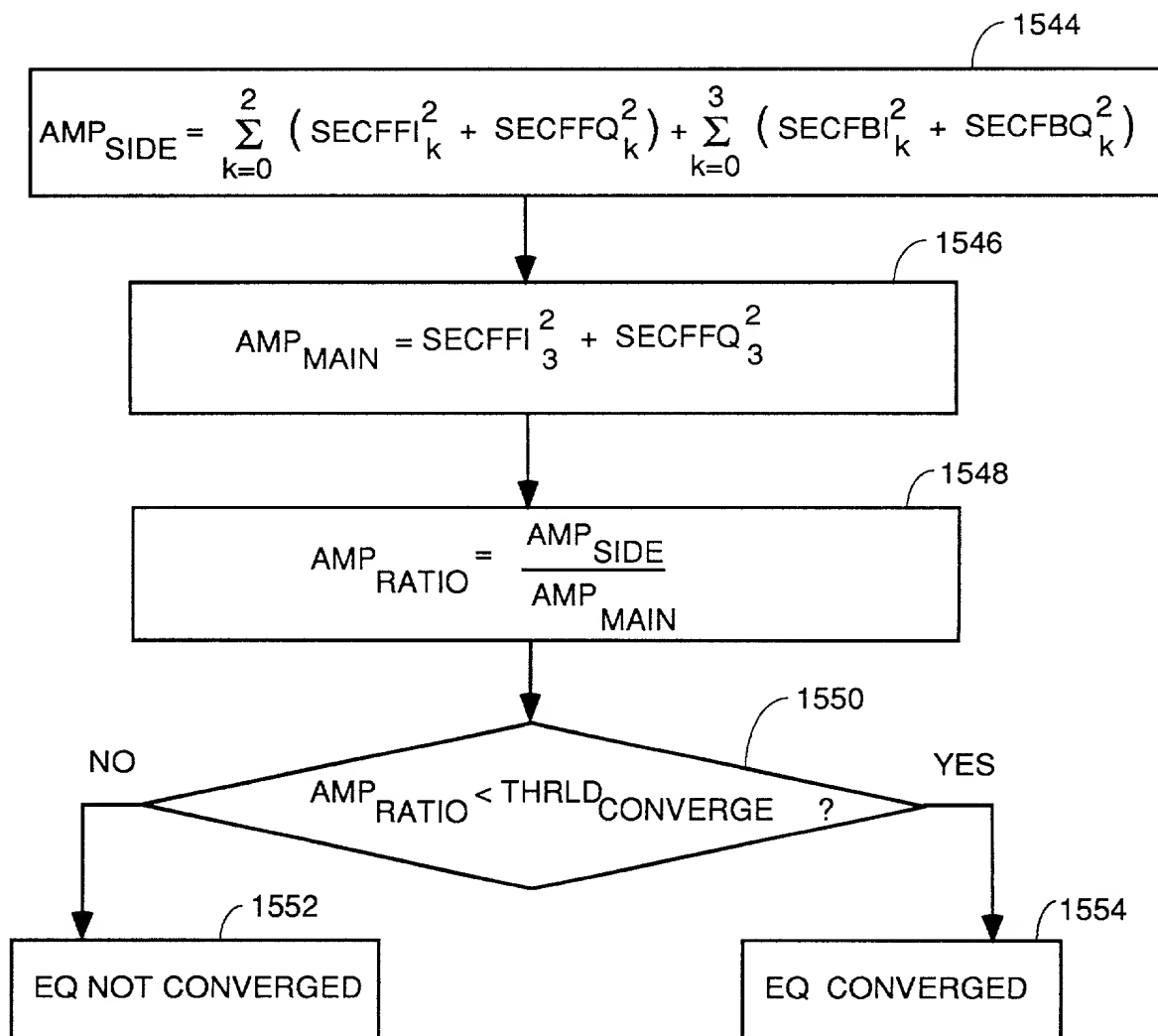


NOTE: $THRLD_{AMP} = TBD$
 $THRLD_{PHASE} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

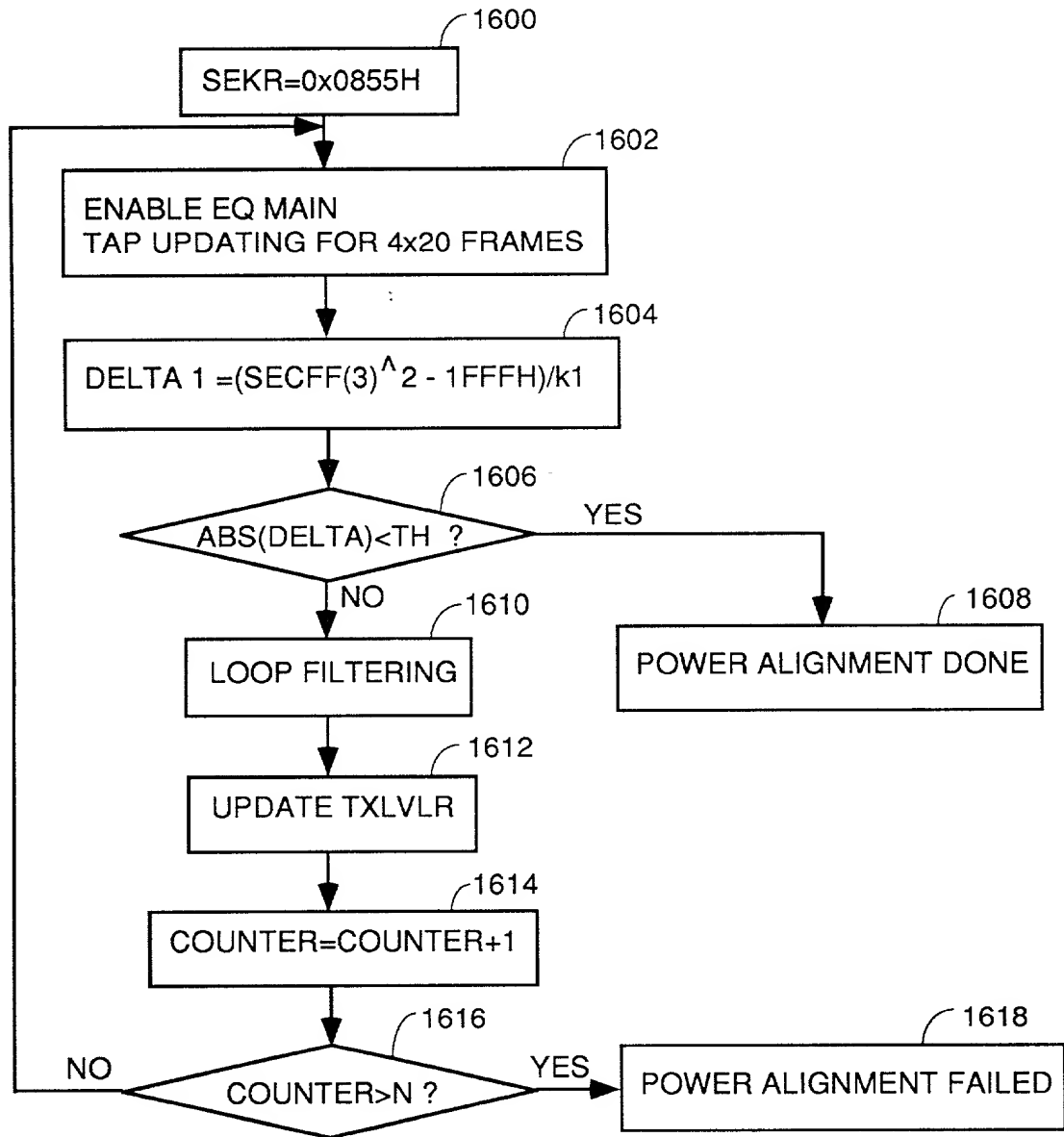
EQ CONVERGENCE CHECK



NOTE: $\text{THRLD}_{\text{CONVERGE}} = 10^{-5}$

FIG. 64

POWER ALIGNMENT FLOW CHART



NOTE: TH = 600H

N = 12

FIG. 65

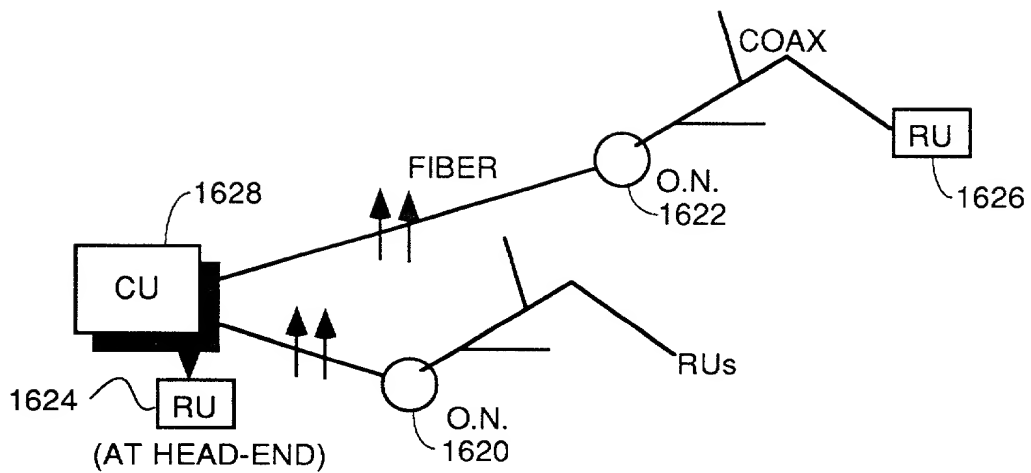
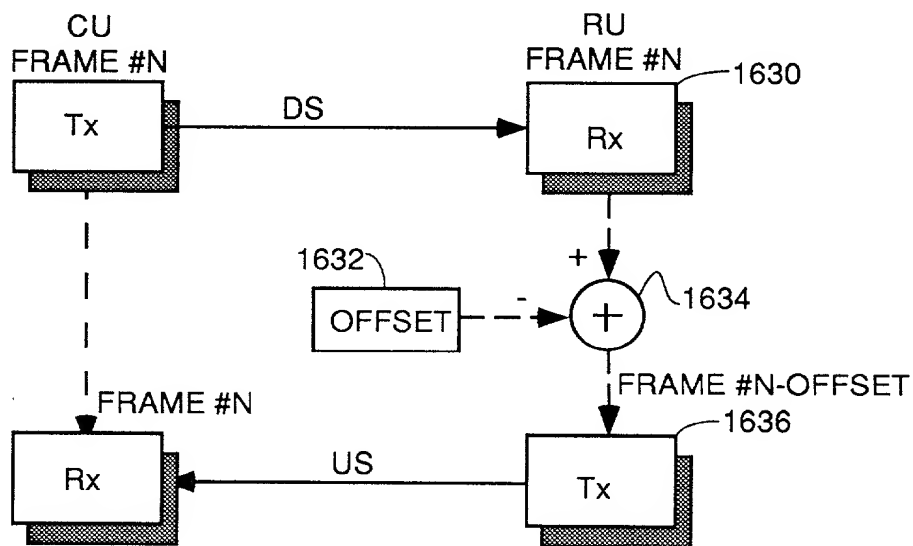


FIG. 66



TOTAL TURN AROUND (TTA) IN FRAMES = OFFSET

FIG. 67

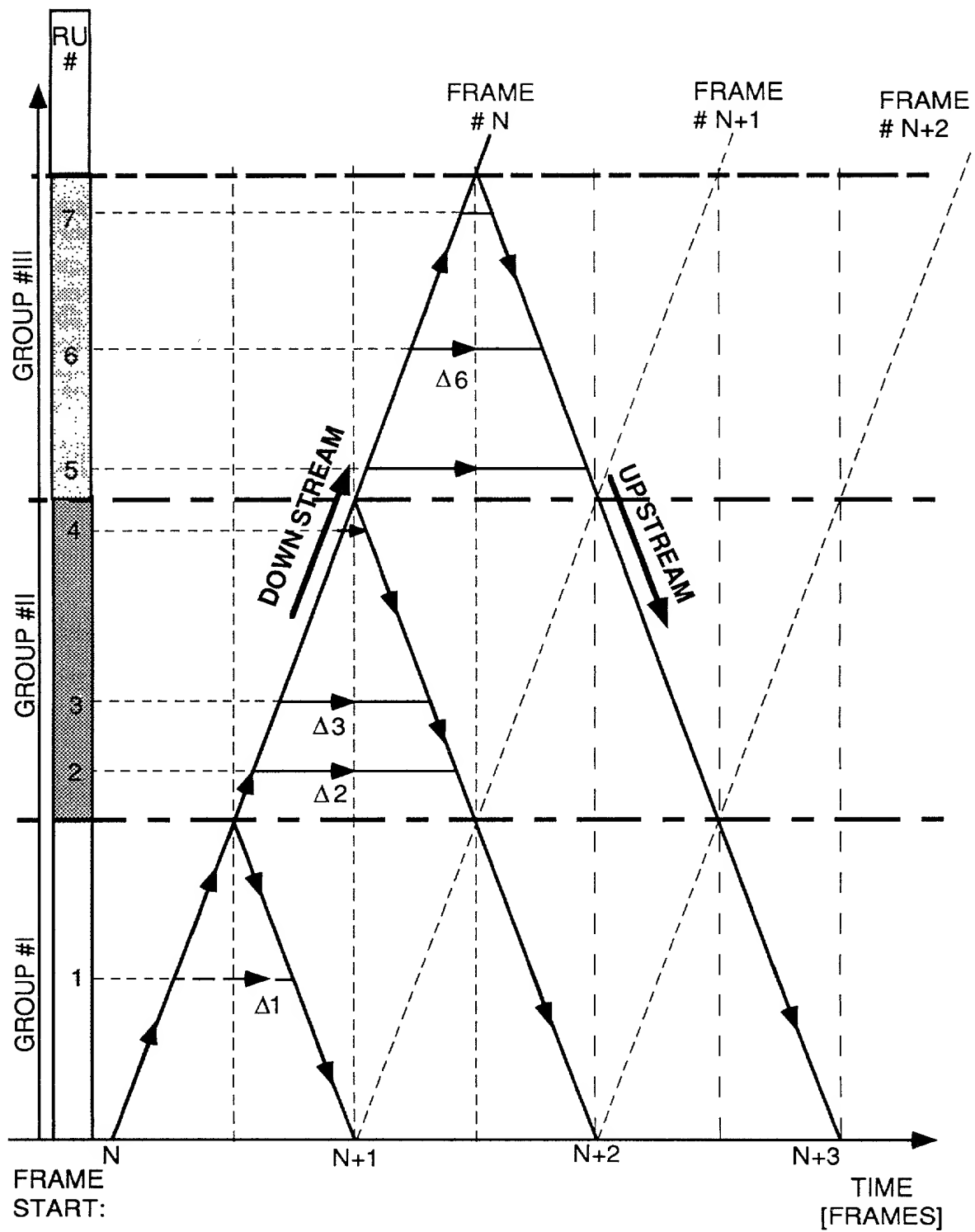
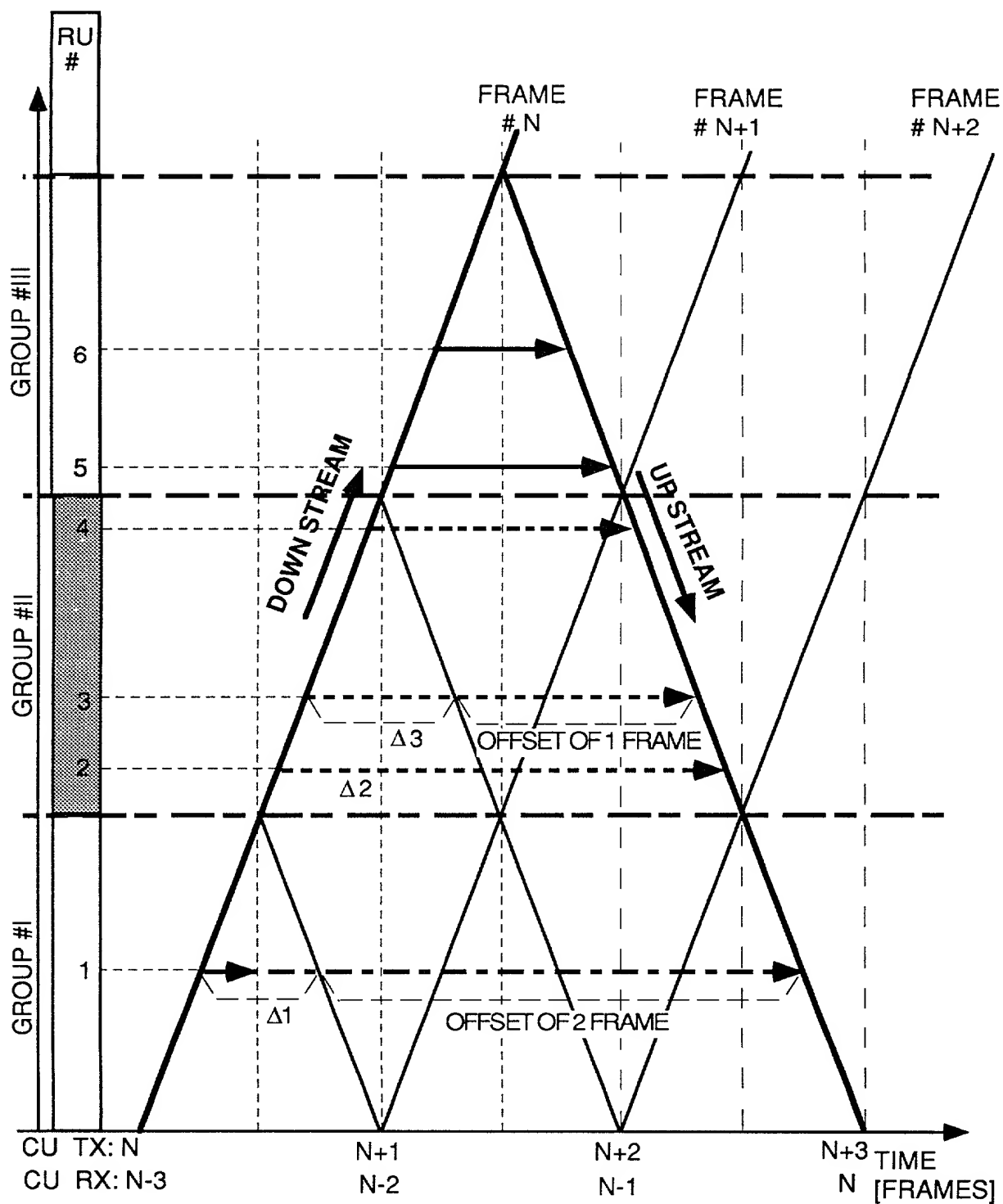


FIG. 68

FIG. 69



CONTROL MESSAGE (DOWNSTREAM) AND FUNCTION (UPSTREAM)
PROPAGATION IN A 3 FRAMES TTA CHANNEL

FIG. 69

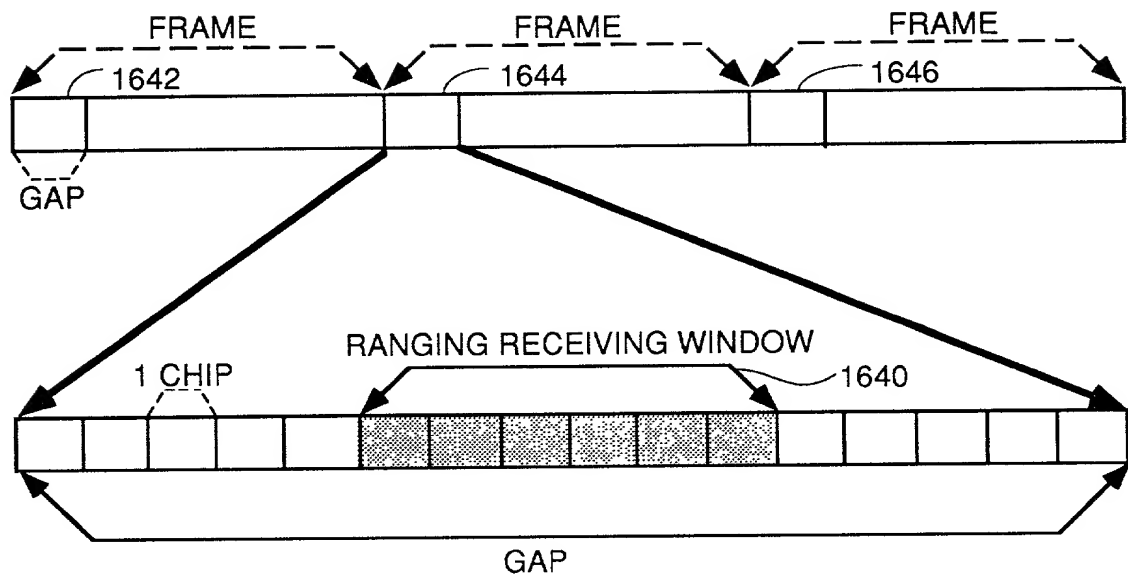
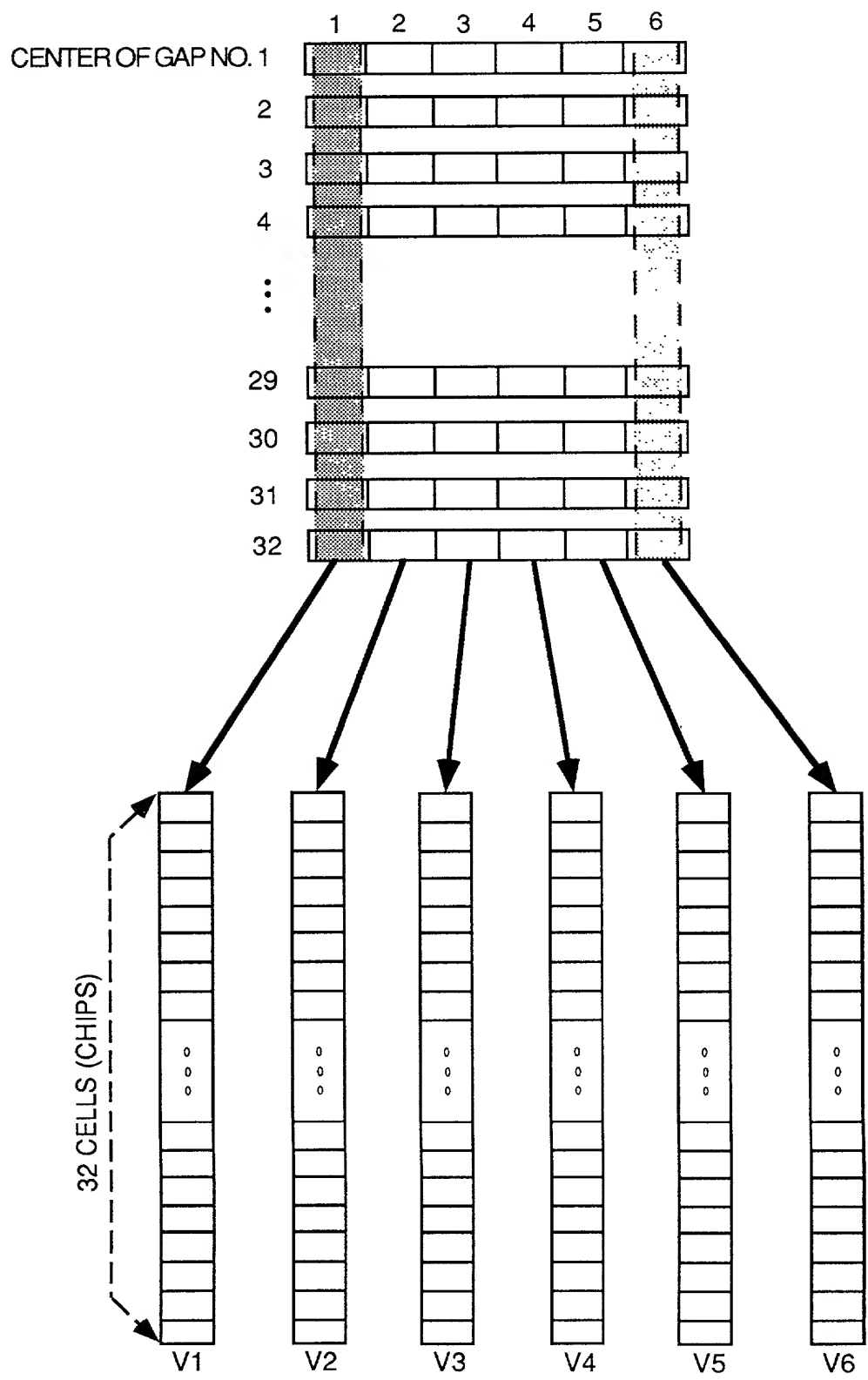


FIG. 70



OVERALL VIEW OF THE CU SENSING WINDOWS
IN A "BOUNDLESS RANGING" ALGORITHM

FIG. 71

CHIP\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	...	0
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72